PLESSEY
Semiconductors

T-51-10-08

SP94308

8-BIT VIDEO SYSTEM ADC

The Plessey SP94308 analog to digital converter has been specially designed for use with NTSC or PAL video signals.

A 1V video signal is AC coupled to the device input, where it is DC clamped, amplified by two and fed through a buffer which drives the ADC input capacitance.

A sync or burst gate pulse can be used to drive the DC clamp circuit. This circuit can be externally adjusted to provide conversion of video only or video and sync.

This analog to digital converter samples the input waveform on the rising edge of the clock and produces a latched output which can be acquired simply by an inverted clock signal.

Also within the SP94308 is an internal clock amplifier and driver. This allows a low level clock signal to be AC coupled directly into the device for applications that may be sensitive to clock radiation.

The clock frequency and analog bandwidth of the SP94308 are compatible with both PAL and NTSC standards where conversion of luma or full composite video signals are required.

FEATURES

- 8 Bits, 20MHz
- ±0.75 LSB Differential Linearity (Typ.)
- No Sample and Hold or Input Buffer Required
- Internal Clock Amplifier
- Internal Clamp Circuit
- Internal Output Latch
- 6MHz Min. Analog Bandwidth
- Output Levels are TTL/CMOS Compatible
- 0°C to 70°C Temperature Range
- Full Static Protection
- On Chip ×2 Amplifier and ADC Buffer

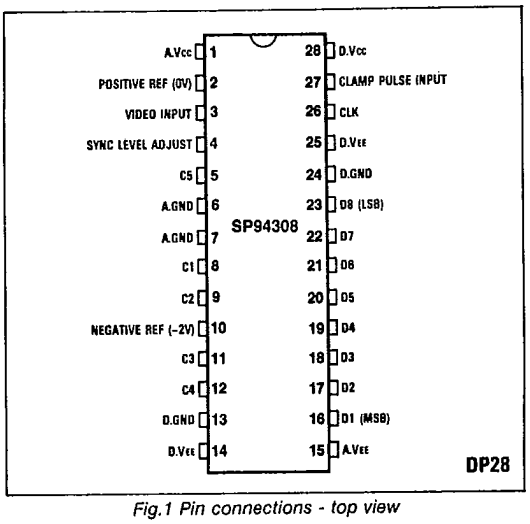

Fig.1 Pin connections - top view

ORDERING INFORMATION

SP94308C DP (Commercial - Plastic DIL package)

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}-V_{EE}	<12V
Output current	<20mA
Storage temperature	-65°C to +150°C
Junction operating temperature	<150°C

THERMAL INFORMATION

Chip to ambient temperature θ_{JA} = 55°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to 70°C, V_{CC} = +5V ± 0.25V, V_{EE} = -5.2V ± 0.25V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current	I_{CC}		35	44	mA	
Negative supply current	I_{EE}		110	150	mA	
Power consumption			750		mW	
Resolution		8			Bits	
Reference current	I_{ref}		12	16	mA	V_{ref} = -2V
Maximum clock rate	fc	20			MHz	
Clock input level		0.25		1.0	V p-p	AC coupled
Analog bandwidth	f_a	6			MHz	Note 3
Input impedance	R_{IN}	100K			Ω	
Differential linearity			±0.75	±1.0	LSB	25°C
Integral linearity				±1.0	LSB	25°C
Differential gain				1.5	%	fc = 20.0MHz
Differential phase			1		Deg	
Logic '1'	V_{IH}	V_{CC}-1.3	V_{CC}-1		V	I_{source} = 1mA
	V_{IH}	V_{CC}-1.1	V_{CC}-0.9		V	I_{source} = 0.1mA
Logic '0'	V_{OL}		0.3	0.4	V	I_{sink} = 1.6mA (Note 2)
Tilt/line			-1.5		mV	100nF input capacitor
Input level			1		V p-p	AC coupled
Sync level adjust output			-1.4		V	Unadjusted (Note 1)
Data valid time	tv		45		ns	At 20MHz clock

NOTES
1. Gain of x2 in input stage.
2. See Fig.7 for equivalent TTL load.
3. Guaranteed but not tested.

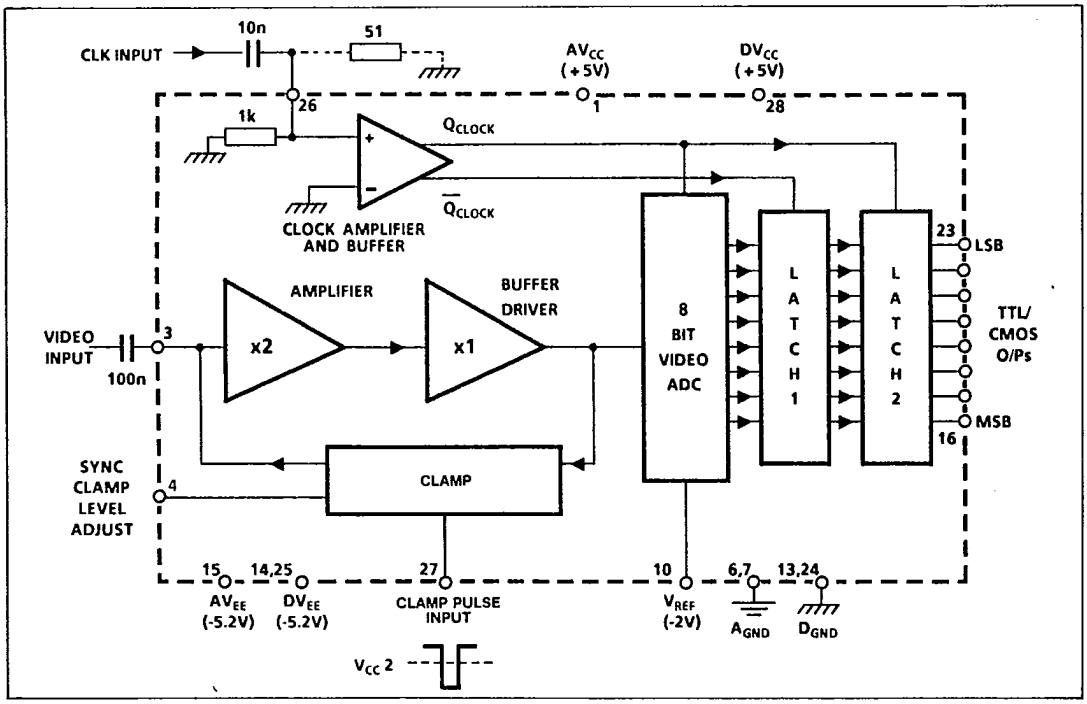

Fig.2 Internal block diagram

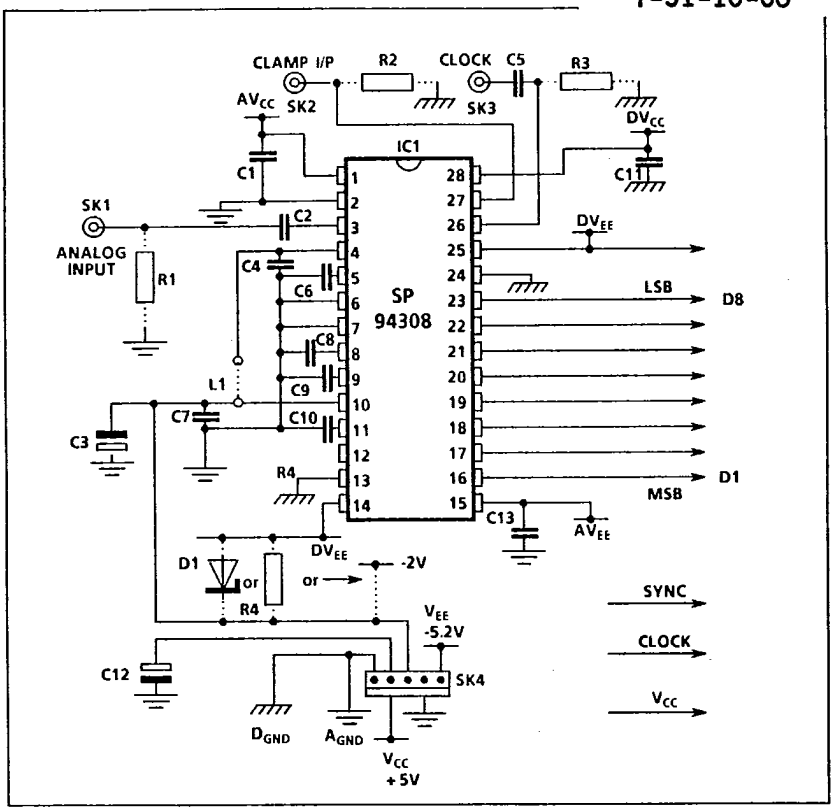

Fig.3 Minimum component application circuit

COMPONENT LIST FOR FIG.4

Resistors

R1	75Ω (optional termination)
R2	47Ω (optional termination)
R3	47Ω (optional termination)
R4	Approx. 560Ω (optional)

Semiconductors

IC1	SP94308
D1	BZX79C3V0 (optional)

Sockets

S1-S3	Sub Vis sockets (optional)
S4	KK Molex socket (optional)

Capacitors for ADC, clamp, bias etc.

C1	100nF (optional decoupling)
C2	100nF (input coupling and line clamp)
C3	47μF (electrolytic decoupling)
C4	100nF (optional decoupling)
C5	100nF (coupling)
C6	27pF at 20MHz or 47pF at 10MHz clock
C7	100nF (decoupling)
C8	100nF (decoupling)
C9	100nF (decoupling)
C10	100nF (decoupling)
C11	100nF (optional decoupling)
C12	47μF (electrolytic decoupling)
C13	100nF (optional decoupling)

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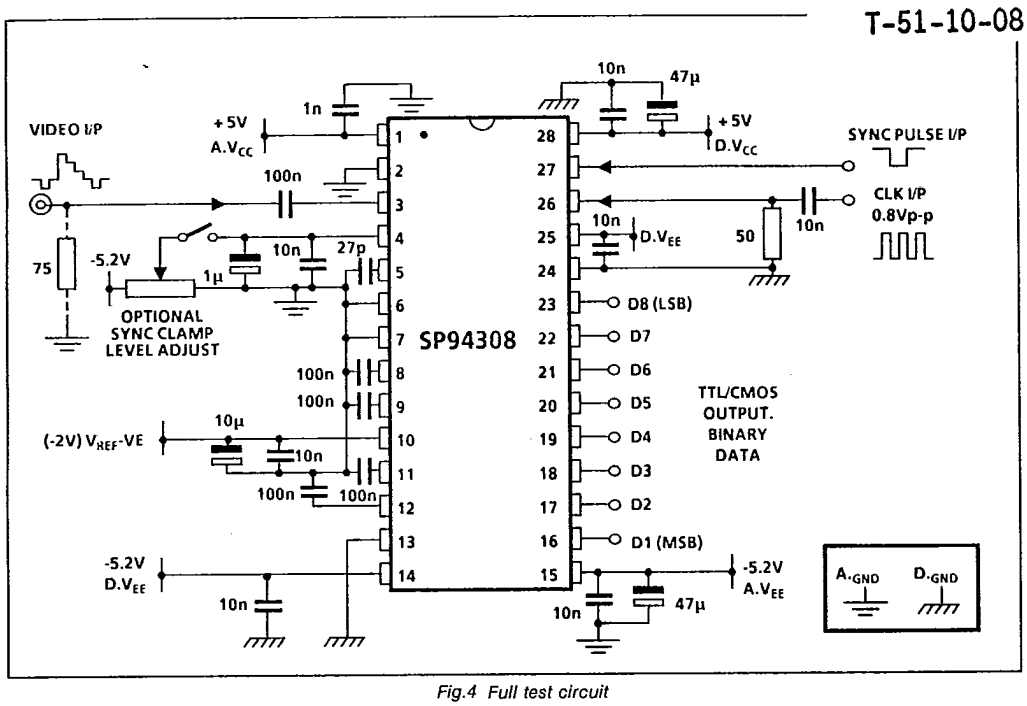

Fig.4 Full test circuit

APPLICATIONS

The SP94308 combines a clamp circuit, sample and hold, x2 amplifier, ADC driver, video ADC and output latch that form a conventional 8-bit video digitising system.

An on-chip clock amplifier allows the device to be clocked from low level sine or square wave signals. This reduces the possibility of patterning due to crosstalk.

The device offers the flexibility for either sync clamping or black level clamping of the video signal.

Sync Clamp

Sync clamping is provided by applying a negative going clamp pulse to pin 27 during the sync period. This pulse should be more than 1.5µs wide and it should cross the internal switching threshold of Vcc/2. Pin 4 should be connected to V_{REF-} (pin 10 -2V) to allow the total video with its sync to be digitised.

Black Level Clamping

This can be achieved by applying a negative clamp pulse to pin 27 within the back porch of the video signal. The clamp pulse should avoid the colour burst - this ensures no attenuation of the burst signal.

The clamping pulse can be derived from a burst gate pulse or by delaying the sync pulse with a dual monostable (SN74123N).

When using a back porch clamping pulse, pin 4 should be decoupled to analog ground using a 100nF capacitor. The device will then self-bias this pin to -1.4V. This provides full digitisation of the video and its sync.

It is also possible to adjust the voltage on pin 4 and reduce the reference voltage pin 10 to provide digitisation of the active video information only.

If a clamp pulse is not readily available within the application it can be generated from the incoming video signal (see circuit shown in Fig.5). The variable resistor RV can be adjusted for different slice levels of the incoming video sync.

The digital outputs of the SP94308 are latched and have a 90% of CLK, data valid time at 20MHz. This allows the 8-Bit TTL output to be acquired simply by an inverse CLK signal. See Fig.6.

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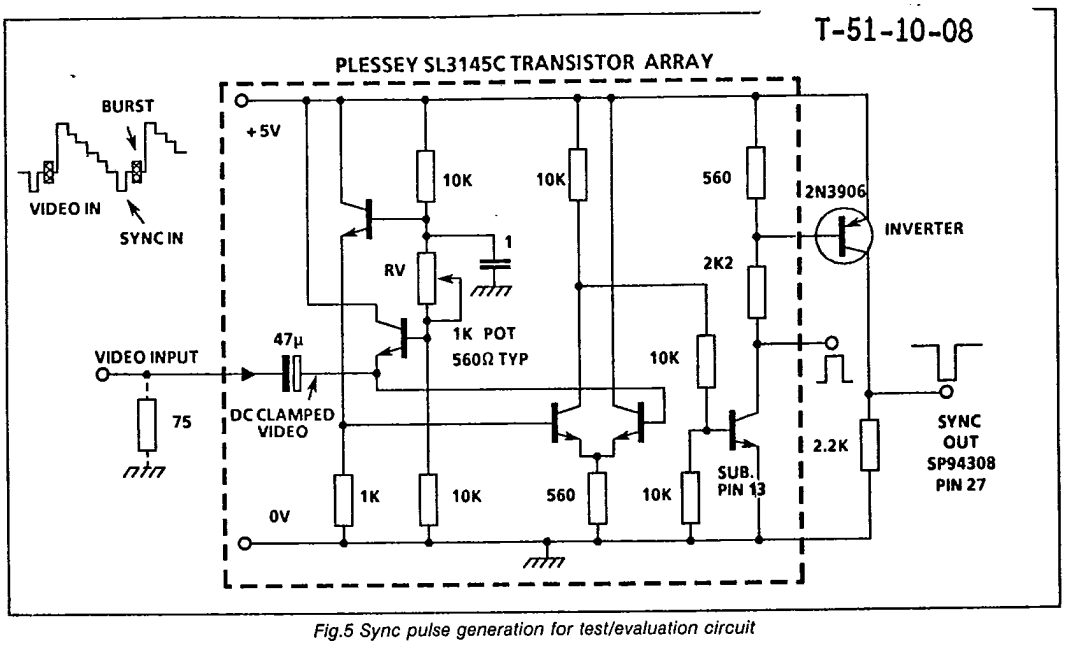

Fig.5 Sync pulse generation for test/evaluation circuit

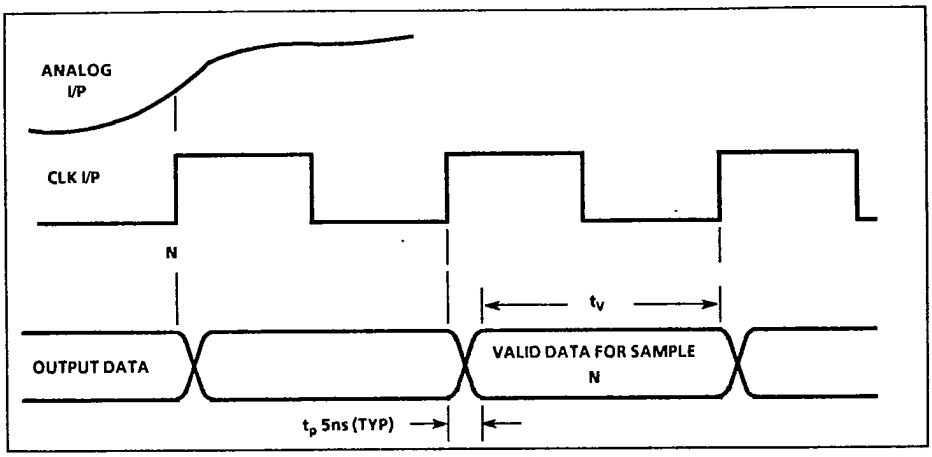

Fig.6 Timing diagram

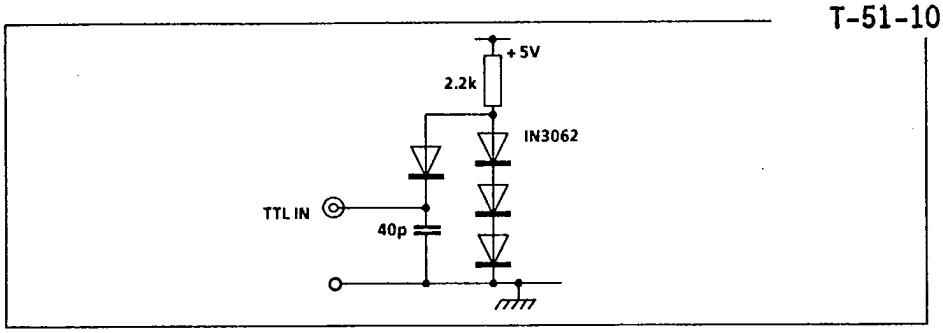

Fig.7 Equivalent TTL test load

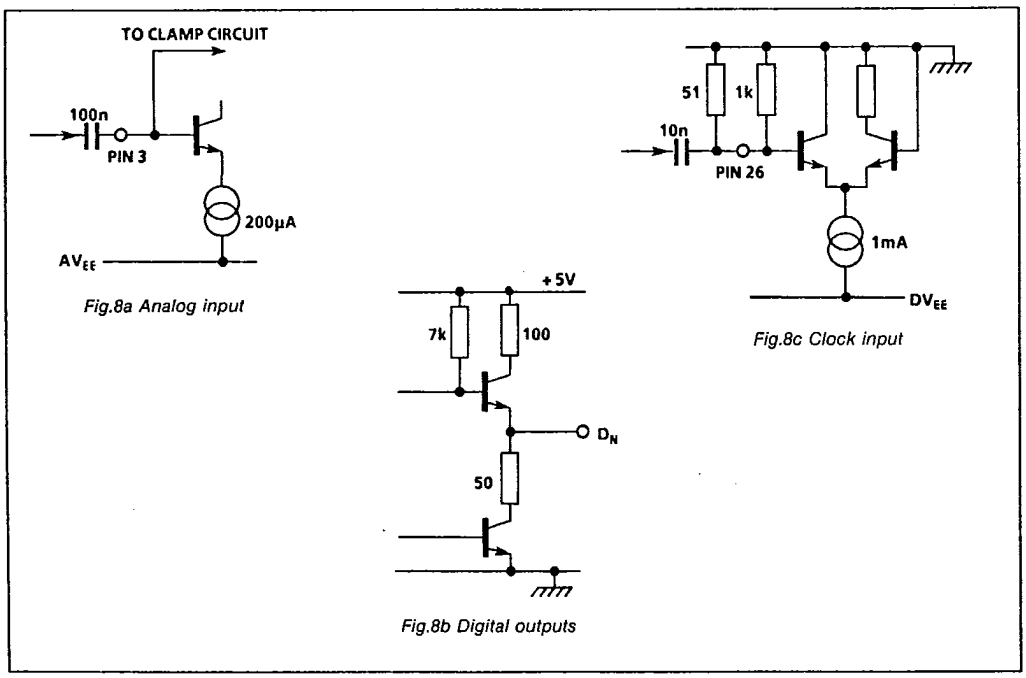

Fig.8a Analog input

Fig.8b Digital outputs

Fig.8c Clock input

Fig.8 Equivalent device inputs and outputs.