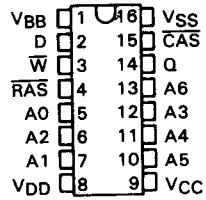
OCTOBER 1977—REVISED NOVEMBER 1985

- 16,384 X 1 Organization
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL Compatible
- Unlatched Three-State Fully TTL-Compatible Output
- Performance Ranges:

| | ACCESS TIME ROW ADDRESS (MAX) | ACCESS TIME COLUMN ADDRESS (MAX) | READ OR WRITE CYCLE (MIN) | READ-MODIFY-WRITE† CYCLE (MIN) |
|---|---|---|---|---|
| TMS4116-15 | 150 ns | 100 ns | 375 ns | 375 ns |
| TMS4116-20 | 200 ns | 135 ns | 375 ns | 375 ns |
| TMS4116-25 | 250 ns | 165 ns | 410 ns | 515 ns |

- Page-Mode Operation for Faster Access Time
- Common I/O Capability with Early Write Feature
- Low-Power Dissipation
  - Operating . . . 462 mW (Max)
  - Standby . . . 20 mW (Max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology
- 16-Pin 300-Mil (7,62-mm) Package Configuration

N PACKAGE
(TOP VIEW)




| PIN NOMENCLATURE | |
|---|---|
| A0-A6 | Addresses |
| $\overline{CAS}$ | Column-Address Strobe |
| D | Data Input |
| Q | Data Output |
| $\overline{RAS}$ | Row-Address Strobe |
| $V_{BB}$ | −5-V Power Supply |
| $V_{CC}$ | 5-V Power Supply |
| $V_{DD}$ | 12-V Power Supply |
| $V_{SS}$ | Ground |
| $\overline{W}$ | Write Enable |



## description

The TMS4116 series is composed of monolithic high-speed dynamic 16,384-bit MOS random-access memories organized as 16,384 one-bit words, and employs single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row-Address Strobe $\overline{RAS}$ (or $\overline{R}$) and Column-Address Strobe $\overline{CAS}$ (or $\overline{C}$). All address lines (A0 through A6) and data in (D) are latched on chip to simplify system design. Data out (Q) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 350 milliwatts active and 6 milliwatts during standby ($V_{CC}$ is not required during standby operation). To retain data, only 10 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS4116 series is offered in a 16-pin dual-in-line plastic (N suffix) package and is guaranteed for operation from 0°C to 70°C. The package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

## operation

### address (A0-A6)

Fourteen address bits are required to decode 1 of 16,384 storage cell locations. Seven row-address bits are set up on pins A0 through A6 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the

†The term "read-write cycle" is sometimes used as an alternative to "read-modify-write cycle."

seven column-address bits are set up on pins A0 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

**write enable ($\overline{W}$)**

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

**data in ($\overline{D}$)**

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

**data out (Q)**

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output goes active after the enable time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

**refresh**

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 128 row addresses (A0 through A6) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

**page mode**

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses on the same page is eliminated. To extend beyond the 128 column locations on a single RAM, the row address and $\overline{RAS}$ is applied to multiple 16K RAMs; $\overline{CAS}$ is decoded to select the proper RAM.

**power up**

$V_{BB}$ must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applies to system use, where failure of the $V_{BB}$ supply must immediately shut down the other supplies. After power up, eight $\overline{RAS}$ cycles must be performed to achieve proper device operation.





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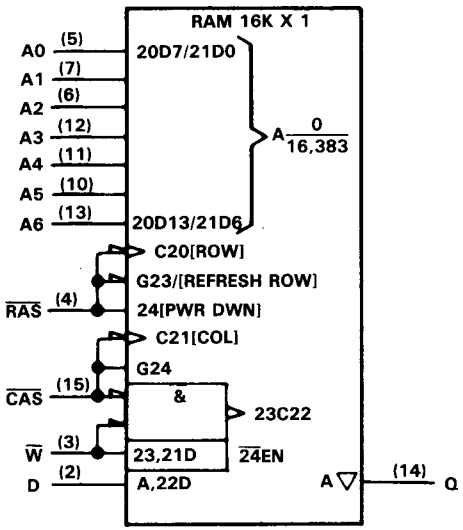
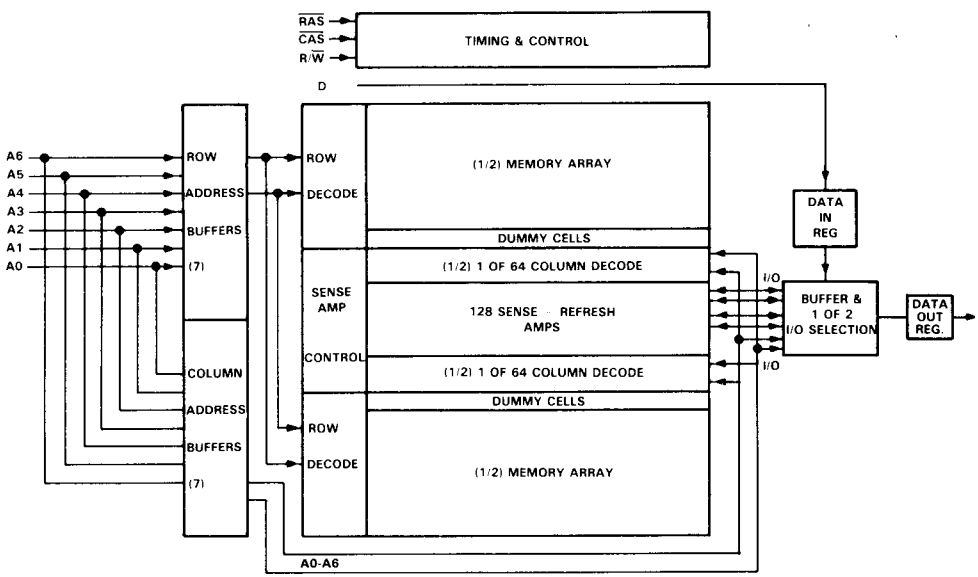
### logic symbol†




†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### functional block diagram



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin (see Note 1) . . . . . −0.5 V to 20 V
Voltage on $V_{CC}$, $V_{DD}$ supplies with respect to $V_{SS}$ . . . . . −1 V to 15 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, $V_{BB}$ (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to $V_{SS}$.



### recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{BB}$ | Supply voltage | | −4.5 | −5 | −5.5 | V |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{DD}$ | Supply voltage | | 10.8 | 12 | 13.2 | V |
| $V_{SS}$ | Supply voltage | | | 0 | | V |
| $V_{IH}$ | High-level input voltage | All inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ | 2.4 | | 7 | V |
| | | $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ | 2.7 | | 7 | |
| $V_{IL}$ | Low-level input voltage (see Note 2) | | −1 | 0 | 0.8 | V |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage only.

## electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −5 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4.2 mA | | | 0.4 | V |
| $I_I$ | Input current (leakage) | $V_I$ = 0 V to 7 V, All other pins = 0 V except $V_{BB}$ = −5 V | | | 10 | μA |
| $I_O$ | Output current (leakage) | $V_O$ = 0 to 5.5 V, $\overline{CAS}$ high | | | ±10 | μA |
| $I_{BB1}$ | Average operating current during read or write cycle | Minimum cycle time | | 50 | 200 | μA |
| $I_{CC1}$‡ | | | | | 4§ | mA |
| $I_{DD1}$ | | | | 27 | 35 | mA |
| $I_{BB2}$ | Standby current | After 1 memory cycle $\overline{RAS}$ and $\overline{CAS}$ high | | 10 | 100 | μA |
| $I_{CC2}$ | | | | | ±10 | μA |
| $I_{DD2}$ | | | | 0.5 | 1.5 | mA |
| $I_{BB3}$ | Average refresh current | Minimum cycle time $\overline{RAS}$ cycling, $\overline{CAS}$ high | | 50 | 200 | μA |
| $I_{CC3}$ | | | | | ±10 | μA |
| $I_{DD3}$ | | | | 20 | 27 | mA |
| $I_{BB4}$ | Average page-mode current | Minimum cycle time $\overline{RAS}$ low, $\overline{CAS}$ cycling | | 50 | 200 | μA |
| $I_{CC4}$‡ | | | | | 4§ | mA |
| $I_{DD4}$ | | | | 20 | 27 | mA |

† All typical values are at $T_A$ = 25°C and nominal supply voltages.
‡ $V_{CC}$ is applied only to the output buffer, so $I_{CC}$ depends on output loading.
§ Output loading two standard TTL loads.

## capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

| PARAMETER | | TYP† | MAX | UNIT |
|---|---|---|---|---|
| $C_{i(A)}$ | Input capacitance, address inputs | 4 | 5 | pF |
| $C_{i(D)}$ | Input capacitance, data input | 4 | 5 | pF |
| $C_{i(RC)}$ | Input capacitance, strobe inputs | 8 | 10 | pF |
| $C_{i(W)}$ | Input capacitance, write enable input | 8 | 10 | pF |
| $C_o$ | Output capacitance | 5 | 7 | pF |

## switching characteristics over recommended supply voltage range and operating free-air temperature range

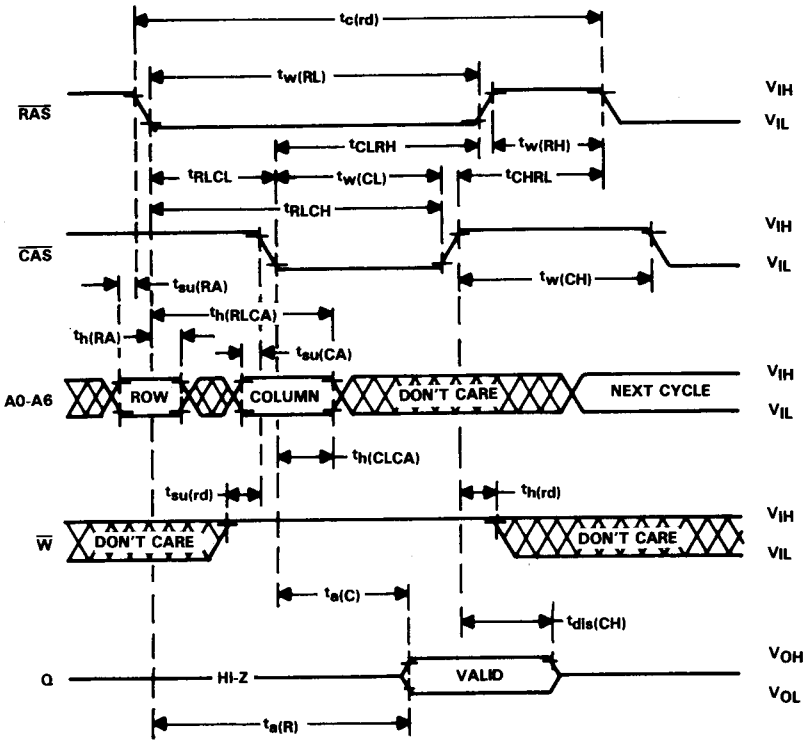
| PARAMETER | | TEST CONDITIONS | ALT. SYMBOL | TMS4116-15 | | TMS4116-20 | | TMS4116-25 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{a(C)}$ | Access time from $\overline{CAS}$ | $C_L$ = 100 pF, Load = 2 Series 74 TTL gates | $t_{CAC}$ | | 100 | | 135 | | 165 | ns |
| $t_{a(R)}$ | Access time from $\overline{RAS}$ | $t_{RLCL}$ = MAX, $C_L$ = 100 pF, Load = 2 Series, 74 TTL gates | $t_{RAC}$ | | 150 | | 200 | | 250 | ns |
| $t_{dis(CH)}$ | Output disable time after $\overline{CAS}$ high | $C_L$ = 100 pF, Load = 2 Series 74 TTL gates | $t_{OFF}$ | 0 | 40 | 0 | 50 | 0 | 60 | ns |

† All typical values are at $T_A$ = 25°C and nominal supply voltages.

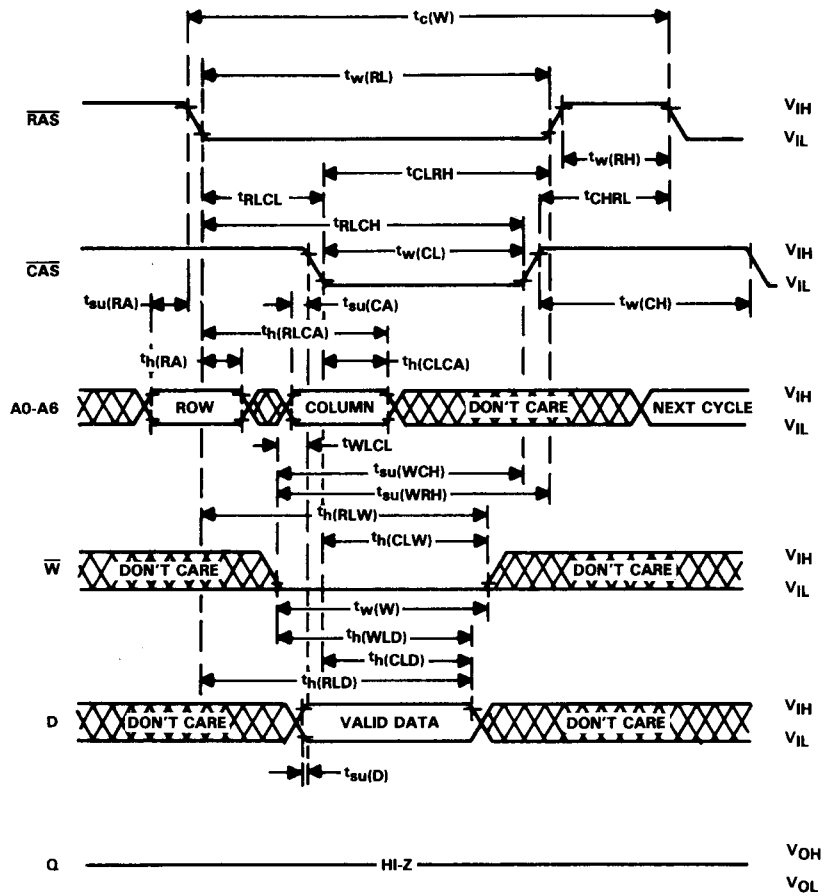
## timing requirements over recommended supply voltage range and operating free-air temperature range

| | | ALT. SYMBOL | TMS4116-15 MIN | TMS4116-15 MAX | TMS4116-20 MIN | TMS4116-20 MAX | TMS4116-25 MIN | TMS4116-25 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{c(P)}$ | Page-mode cycle time | $t_{PC}$ | 170 | | 225 | | 275 | | ns |
| $t_{c(rd)}$ | Read cycle time | $t_{RC}$ | 375 | | 375 | | 410 | | ns |
| $t_{c(W)}$ | Write cycle time | $t_{WC}$ | 375 | | 375 | | 410 | | ns |
| $t_{c(rdW)}$ | Read-modify-write cycle time | $t_{RWC}$ | 375 | | 375 | | 515 | | ns |
| $t_{w(CH)}$ | Pulse duration, $\overline{CAS}$ high (precharge time) | $t_{CP}$ | 60 | | 80 | | 100 | | ns |
| $t_{w(CL)}$ | Pulse duration, $\overline{CAS}$ low | $t_{CAS}$ | 100 | 10,000 | 135 | 10,000 | 165 | 10,000 | ns |
| $t_{w(RH)}$ | Pulse duration, $\overline{RAS}$ high (precharge time) | $t_{RP}$ | 100 | | 120 | | 150 | | ns |
| $t_{w(RL)}$ | Pulse duration, $\overline{RAS}$ low | $t_{RAS}$ | 150 | 10,000 | 200 | 10,000 | 250 | 10,000 | ns |
| $t_{w(W)}$ | Write pulse duration | $t_{WP}$ | 45 | | 55 | | 75 | | ns |
| $t_t$ | Transition times (rise and fall) for $\overline{RAS}$ and CAS | $t_T$ | 3 | 35 | 3 | 50 | 3 | 50 | ns |
| $t_{su(CA)}$ | Column-address setup time | $t_{ASC}$ | −10 | | −10 | | −10 | | ns |
| $t_{su(RA)}$ | Row-address setup time | $t_{ASR}$ | 0 | | 0 | | 0 | | ns |
| $t_{su(D)}$ | Data setup time | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| $t_{su(rd)}$ | Read-command setup time | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| $t_{su(WCH)}$ | Write-command setup time before $\overline{CAS}$ high | $t_{CWL}$ | 60 | | 80 | | 100 | | ns |
| $t_{su(WRH)}$ | Write-command setup time before $\overline{RAS}$ high | $t_{RWL}$ | 60 | | 80 | | 100 | | ns |
| $t_{h(CLCA)}$ | Column-address hold time after $\overline{CAS}$ low | $t_{CAH}$ | 45 | | 55 | | 75 | | ns |
| $t_{h(RA)}$ | Row-address hold time | $t_{RAH}$ | 20 | | 25 | | 35 | | ns |
| $t_{h(RLCA)}$ | Column-address hold time after $\overline{RAS}$ low | $t_{AR}$ | 95 | | 120 | | 160 | | ns |
| $t_{h(CLD)}$ | Data hold time after $\overline{CAS}$ low | $t_{DHC}$ | 45 | | 55 | | 75 | | ns |
| $t_{h(RLD)}$ | Data hold time after $\overline{RAS}$ low | $t_{DHR}$ | 95 | | 120 | | 160 | | ns |
| $t_{h(WLD)}$ | Data hold time after $\overline{W}$ low | $t_{DHW}$ | 45 | | 55 | | 75 | | ns |
| $t_{h(rd)}$ | Read-command hold time | $t_{RCH}$ | 0 | | 0 | | 0 | | ns |
| $t_{h(CLW)}$ | Write-command hold time after $\overline{CAS}$ low | $t_{WCH}$ | 45 | | 55 | | 75 | | ns |
| $t_{h(RLW)}$ | Write-command hold time after $\overline{RAS}$ low | $t_{WCR}$ | 95 | | 120 | | 160 | | ns |
| $t_{RLCH}$ | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high | $t_{CSH}$ | 150 | | 200 | | 250 | | ns |
| $t_{CHRL}$ | Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low | $t_{CRP}$ | −20 | | −20 | | −20 | | ns |
| $t_{CLRH}$ | Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high | $t_{RSH}$ | 100 | | 135 | | 165 | | ns |
| $t_{CLWL}$ | Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only) | $t_{CWD}$ | 70 | | 95 | | 125 | | ns |
| $t_{RLCL}$ | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time) | $t_{RCD}$ | 20 | 50 | 25 | 65 | 35 | 85 | ns |
| $t_{RLWL}$ | Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write-cycle only) | $t_{RWD}$ | 120 | | 160 | | 200 | | ns |
| $t_{WLCL}$ | Delay time, W low to $\overline{CAS}$ low (early write cycle) | $t_{WCS}$ | −20 | | −20 | | −20 | | ns |
| $t_{rf}$ | Refresh time interval | $t_{REF}$ | | 2 | | 2 | | 2 | ms |

## read cycle timing



**early write cycle timing**



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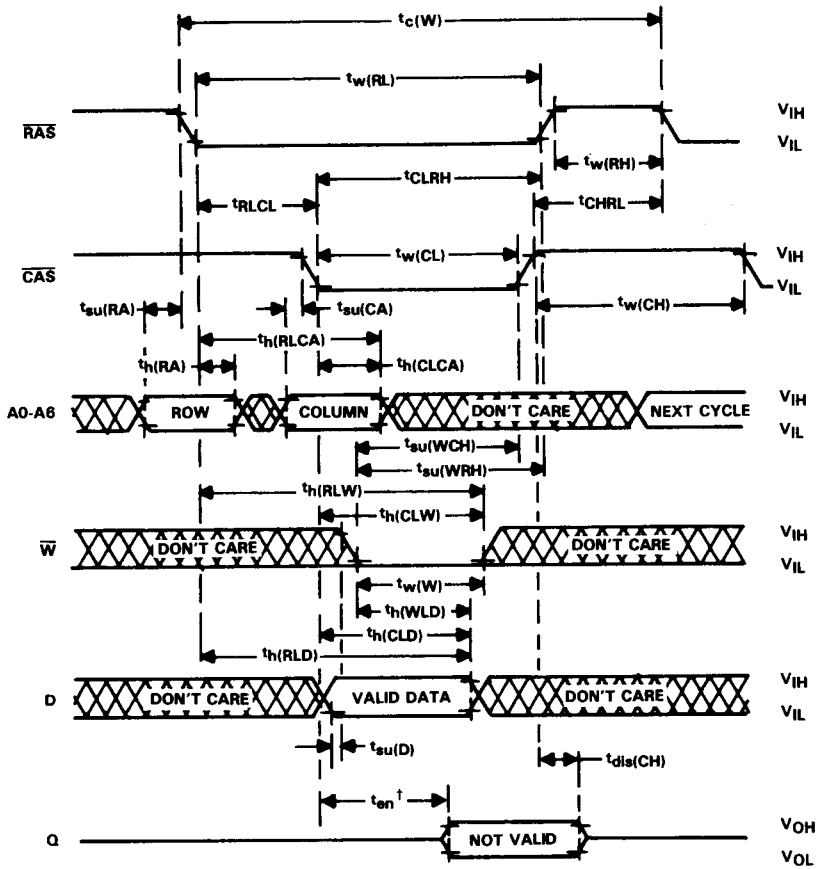
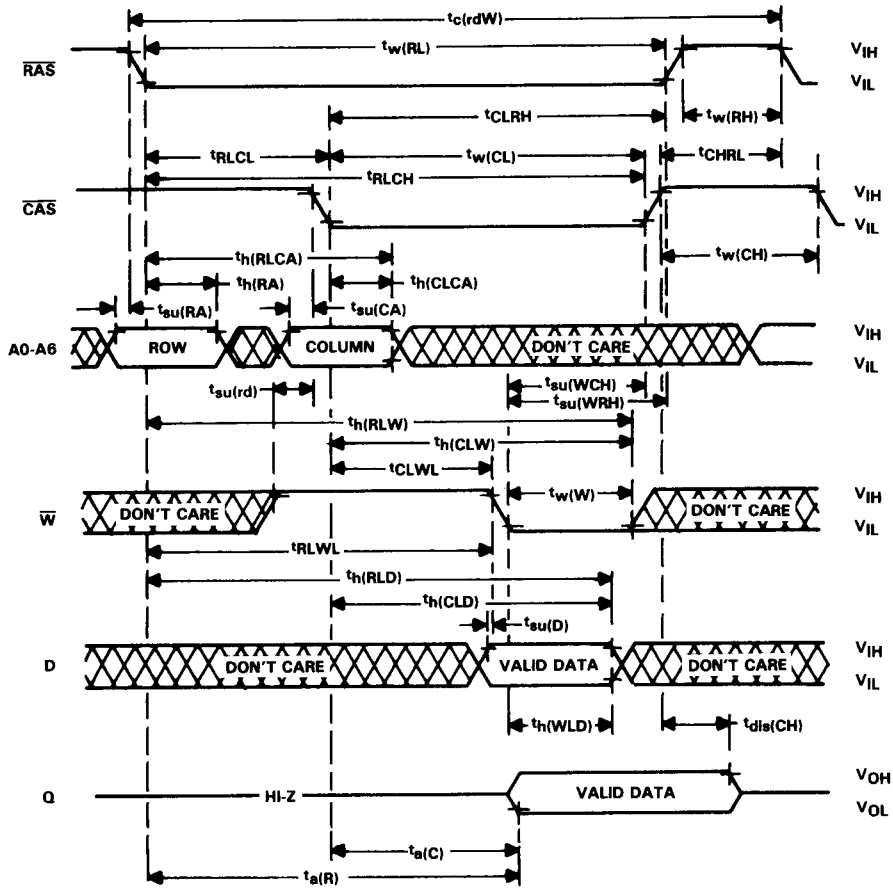
**write cycle timing**

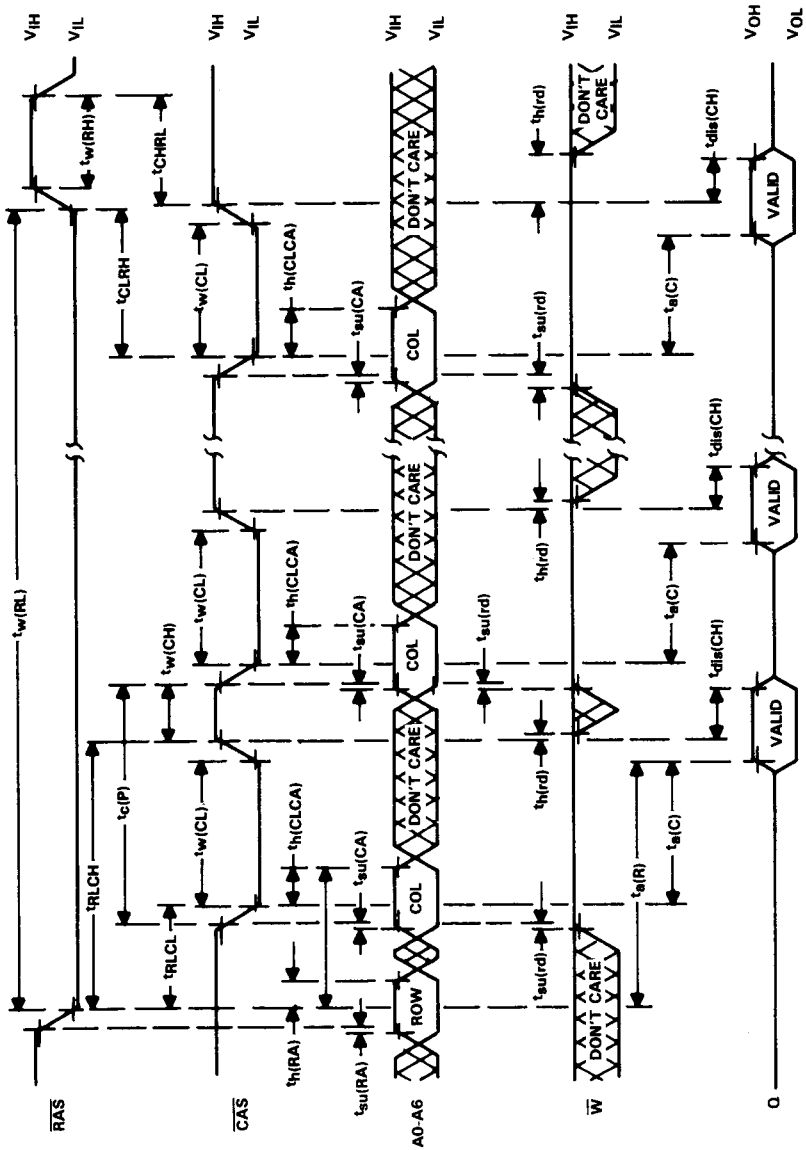



† The enable time ($t_{en}$) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the same active levels at the output are invalid.

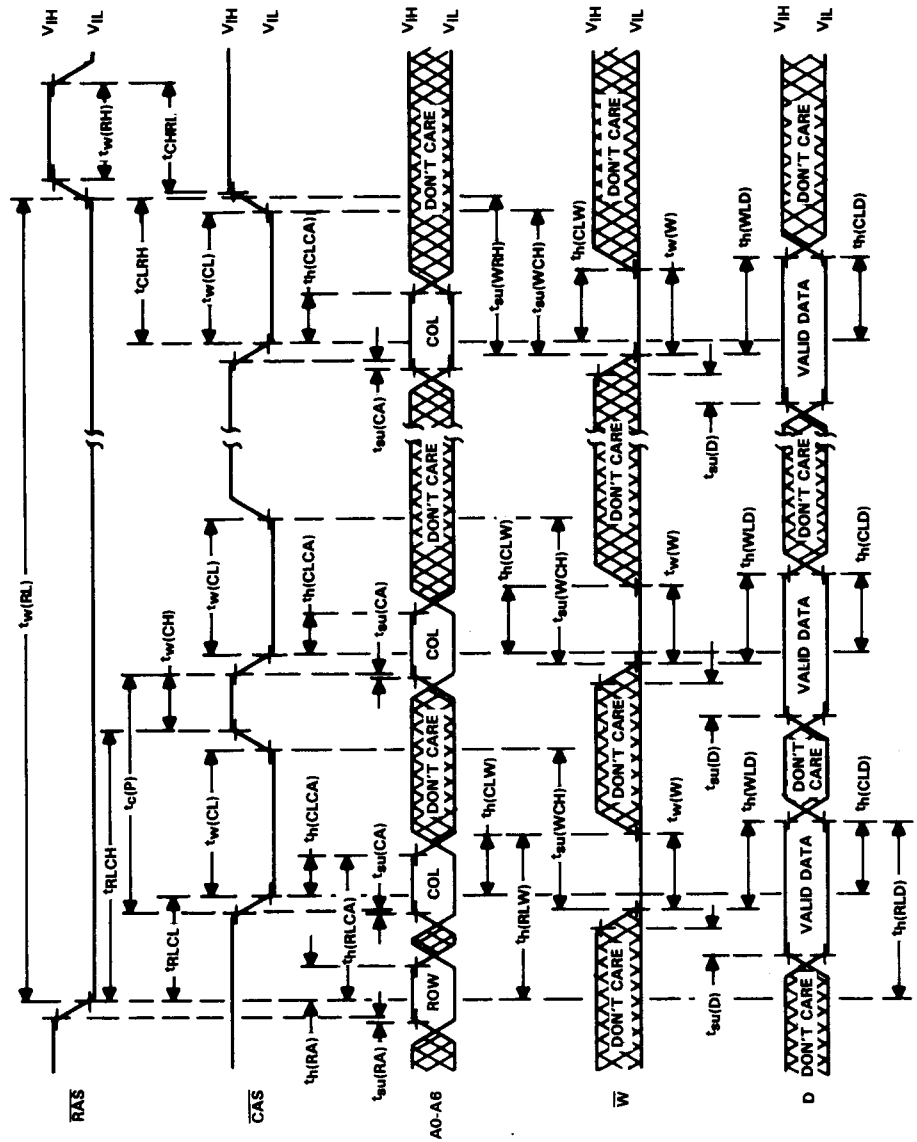
## read-write/read-modify-write cycle timing



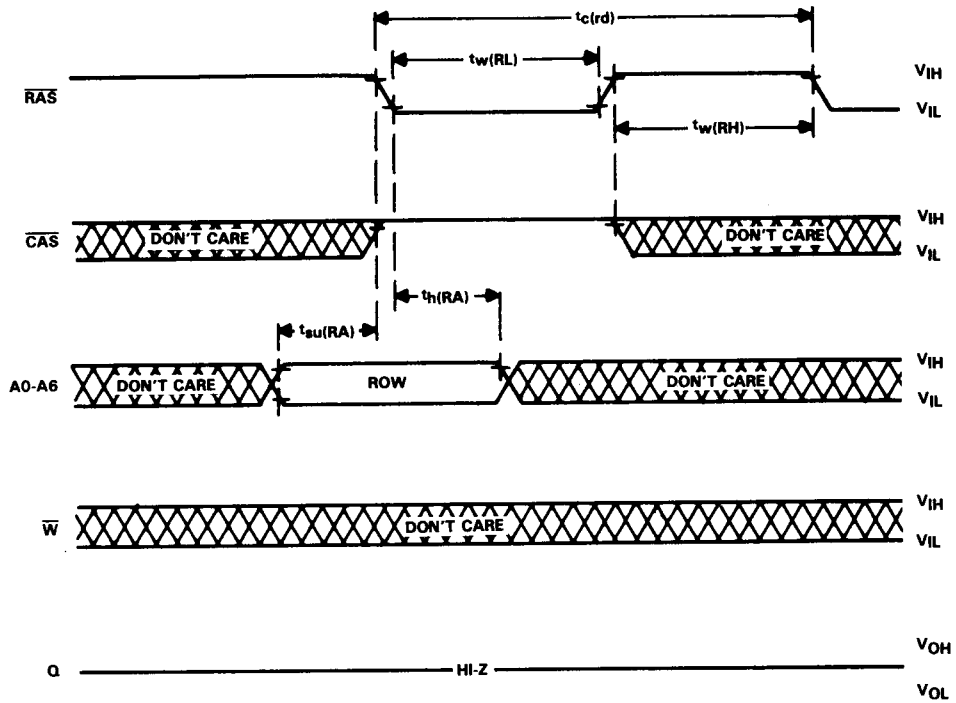
page-mode read cycle timing



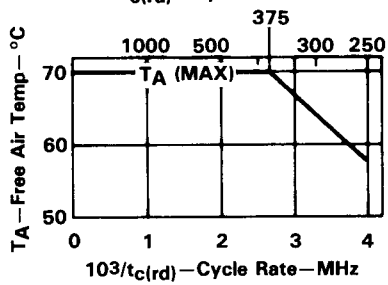
**page-mode write cycle timing**



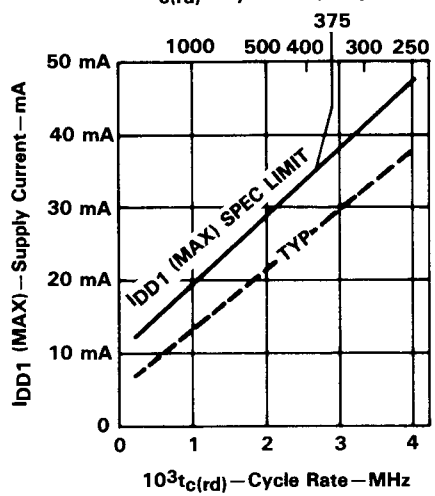
## $\overline{\text{RAS}}$-only refresh timing



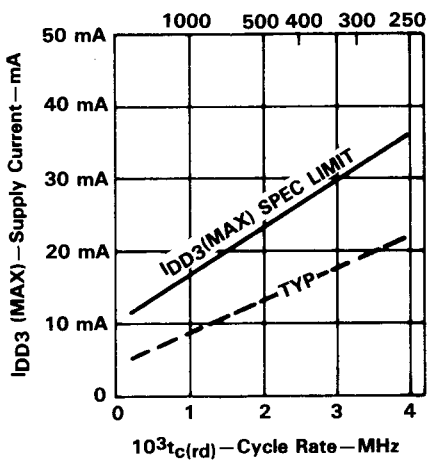
CYCLE RATE (& TIME)
vs
TEMPERATURE




CYCLE RATE (& TIME)
vs
MAX SUPPLY CURRENT, $I_{DD1}$




CYCLE RATE (& TIME)
vs
MAX SUPPLY CURRENT, $I_{DD3}$




PAGE-MODE CYCLE RATE (& TIME)
vs
MAX SUPPLY CURRENT, $I_{DD4}$