

MSM3864RS

8,192 WORD x 8 BIT MASK ROM

GENERAL DESCRIPTION

The MSM3864RS is an N-channel silicon gate MOS device MASK ROM with a 8,192 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

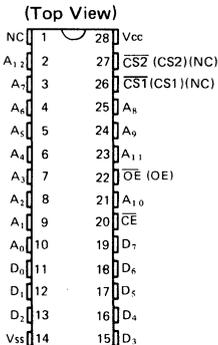
As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expansion of memory and bus line control.

FEATURES

- 5V single power supply
- 8,192 words x 8 bits
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



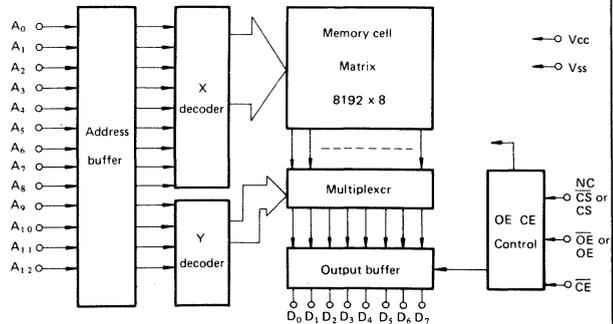
PIN CONFIGURATION



OE : Output enable
 Vcc, Vss : Power supply
 A₀ ~ A₁₂ : Address input
 D₀ ~ D₇ : Data output
 CE : Chip enable
 CS₁, CS₂ : Chip select

Note: Please specify the OE active level and CS active level or open in ordering this IC.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V _{cc}	-0.5 to 7	V	Respect to V _{ss}
Input Voltage	V _I	-0.5 to 7	V	Respect to V _{ss}
Output Voltage	V _O	-0.5 to 7	V	Respect to V _{ss}
Power Dissipation	P _D	1	W	Per package
Operating Temperature	T _{opr}	0 to 70	°C	
Storage Temperature	T _{stg}	-55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V _{cc}	—	4.5	5	5.5	V
	V _{ss}	—	0	0	0	V
Input Signal Level	V _{IH}	—	2	5	6	V
	V _{IL}	—	-0.5	0	0.8	V
Output Signal Level	V _{OH}	I _{OH} = -400 μA	2.4	—	V _{cc}	V
	V _{OL}	I _{OL} = 2.1 mA	—	—	0.4	V
Input Leakage Current	I _{LI}	V _I = 0V or V _{cc}	-10	—	10	μA
Output Leakage Current	I _{LO}	V _O = 0V or V _{cc} Chip not selected	-10	—	10	μA
Power Supply Current	I _{cc}	V _{cc} = Max. I _O = 0 mA	—	—	100	mA
	I _{ccs}	V _{cc} = Max. CE = V _{IH} , I _O = 0 mA	—	—	30	mA
Peak Power ON Current	I _{po}	V _{cc} = GND ~ V _{cc} Min. CE = V _{cc} or V _{IH}	—	—	60	mA
Operating Temperature	T _{opr}	—	0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

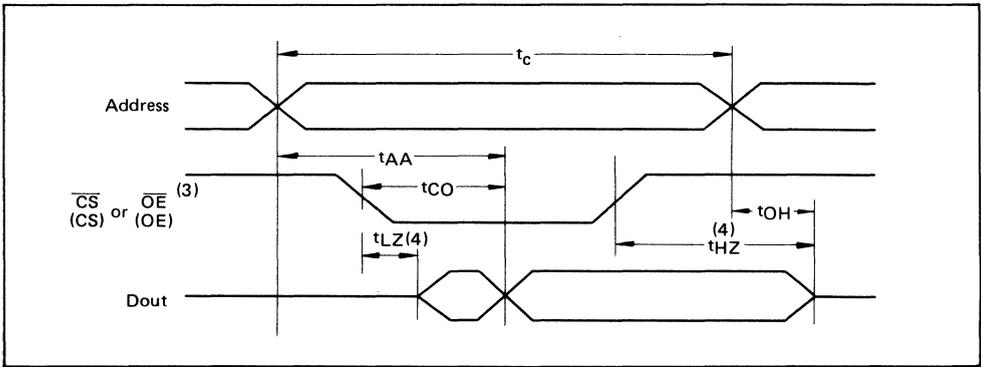
Parameter	Conditions
Input Signal Level	V _{IH} =2.4V V _{IL} =0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C _L =100 pF + 1 TTL

READ CYCLE

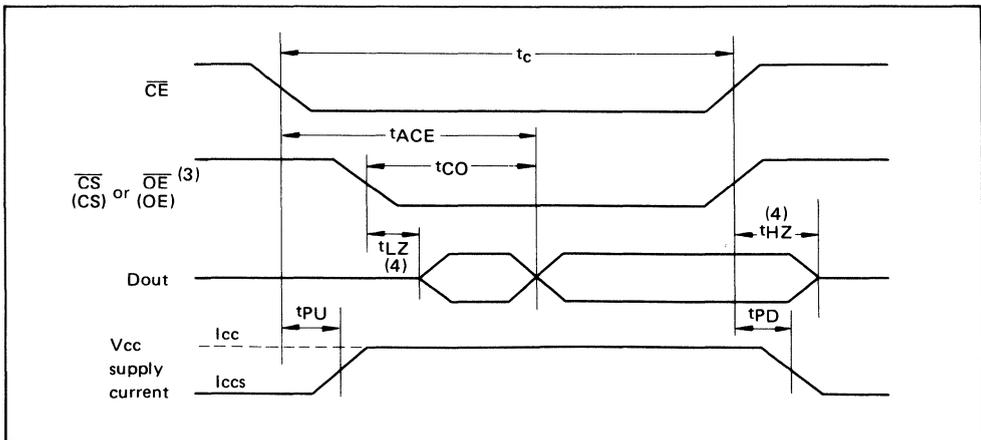
($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0^\circ C$ to $+70^\circ C$)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	250	—		ns	
Address Access Time	t_{AA}	—	—	250	ns	
Chip Enable Access Time	t_{ACE}	—	—	250	ns	
Output Delay Time	t_{CO}	—	—	100	ns	
Output Setting Time	t_{LZ}	10	—	—	ns	
Output Disable Time	t_{HZ}	10	—	100	ns	
Output Retaining Time	t_{OH}	10	—	—	ns	
Power Up Time	t_{PU}	0	—	—	ns	
Power Down Time	t_{PD}	—	—	100	ns	

1) READ CYCLE-1⁽¹⁾



2) READ CYCLE-2⁽²⁾



- Notes:** (1) \overline{CE} is "L" level.
 (2) The address is decided at the same time as or ahead of \overline{CE} "L" level.
 (3) The \overline{OE} and \overline{CS} are shown in the negative logic here, however the active level is freely selected.
 (4) t_{Lz} is determined by the later level, \overline{CE} "L"/ \overline{CS} "L" or \overline{OE} "L".
 t_{Hz} is determined by the earlier \overline{CE} "H"/ \overline{CS} "H" or \overline{OE} "H".
 While, t_{Hz} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	$V_I=0V$
Output Capacitance	C_O		10	pF	$V_O=0V$