32MHz oscillator for 16Mhz MTXPlus+

X1

TCXO3

Default

JP1

JP2

(Optional)

SQW

CLOCK

(Optional)

LTC6900

LTC6905 U7

C7 0.1uF

Divisor

/1

/2 (Open)

/4

JP3

Div Select

10K VR1

10K R20

LTC690x option for overclocking

A fixed 10k R20, with a 10k VR1 and JP2 2–3 gives a range of 21–42Mhz for the system clock input, giving a range of 11–21MHz for PHI – the likely limit of MTXPlus+

(The CPLD clock division logic is optimised for 16MHz PHI and would need to be modified for other speeds)

(Input Clock adjustable between 17 and 170 MHz)

(10K < VR1 < 25K)

CPU CTC RAM ROM RTC 273

C1 C2 C3 C4 C5 C6 0.1uF

D1 LED

330R R1

U1

Z80-CPU

JP6

R2 4.7K

R3 R4 R5 R6 1K

U2

Z80-CTC_DS

R7 4K7

U4

CP/M ROM (Colour or Mono)

27C010

RP1 10K

U3

SRAM_512KO

U6

Page Port

74HC273

U5

DS12887

Intel (Default)

Motorola

Bus Select JP4

JP5

RESET

R8 10k

(Default) (Open)

J0

C96ABC_MTXP

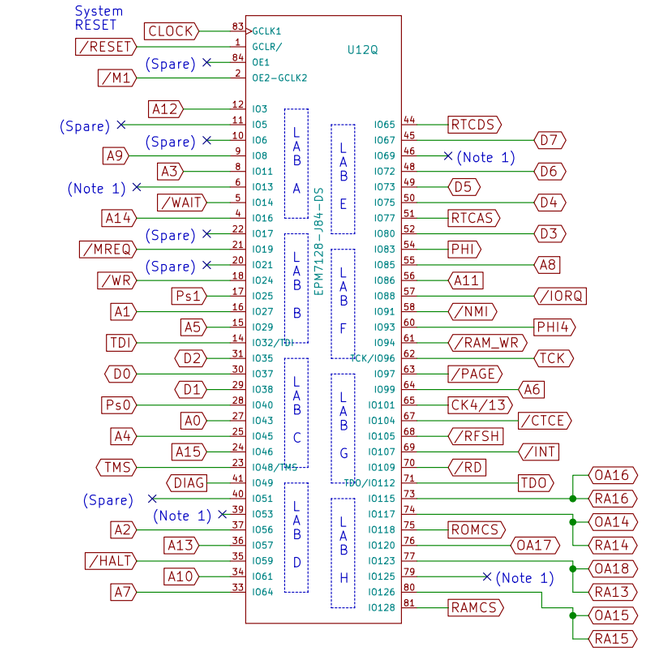
PWR_FLAG

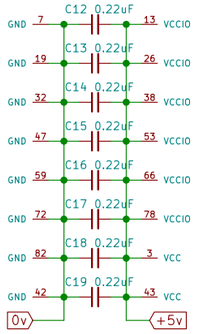
VSS GND VDD Vcc

(+3.3v)

Sheet: /	
File: CPU_Ver230.sch	
Title: MTXPlus+ CPU Board –	
Size: A3	Date: 2016-04-02
KiCad E.D.A. kicad 4.0.1-stable	Id: 1/2

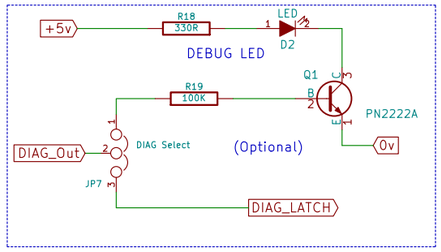
Rev: 2.30

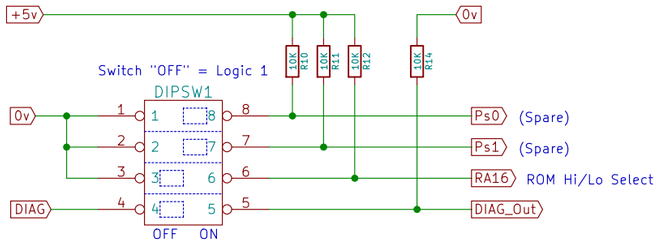




SPECULATOR+ SUPPORT

N/C	OPTIONAL		REQUIRED	
/BUSRQ	/WAIT	✓	/M1	✓
/BUSAK	/HALT	✓	/RD	✓
			/MREQ	✓
			/IORQ	✓
			/RESET	✓
			/INT	✓
			/WR	✓
			/NMI	✓
			/RFSH	✓
			A12	✓
			A11	✓
			A10	✓
			A9	✓
			A8	✓
			A13..A15	✓
			A0..A7	✓
			D0..D7	✓





	EPM7128SLC84	EPM7160SLC84
Input / GLCK1	83	83
Input / GLCLRn	1	1
Input / OE1	84	84
Input / OE2 / GLCK2	2	2
TDI	14	14
TMS	23	23
TCk	62	62
TDO	71	71
GDINT	42, 82	Ground
GNDIO	7, 19, 32, 47, 59, 72	7, 19, 32, 42, 47, 59, 72, 82
VCCINT	3, 43	3, 43
VCCIO	13, 26, 38, 53, 66, 78	13, 26, 38, 53, 66, 78
NC	-	6, 39, 46, 79
User I/O	64	60
LAB A	12, 11, 10, 9, 8, 6, 5, 4	11, 10, 9, 8, 5, 4
LAB B	22, 21, 20, 18, 17, 16, 15, 14	18, 17, 16, 15, 14, 12
LAB C	31, 30, 29, 28, 27, 25, 24, 23	25, 24, 23, 20, 21, 22
LAB D	41, 40, 39, 37, 36, 35, 34, 33	33, 31, 30, 29, 28, 27
LAB E	44, 45, 46, 48, 49, 50, 51, 52	41, 40, 37, 36, 35, 34
LAB F	54, 55, 56, 57, 58, 60, 61, 62	44, 45, 48, 49, 50, 51
LAB G	63, 64, 65, 67, 68, 69, 70, 71	52, 54, 55, 56, 57, 58
LAB H	73, 74, 75, 76, 77, 79, 80, 81	60, 61, 62, 65, 64, 63
LAB I	N/A	67,68,69,70, 71,73
LAB J	N/A	74, 75, 76, 77, 80, 81

MEMORY ADDRESS DECODING

ROM	RAM	PIN
OA18	n/a	A13
OA14	OA14	A14
OA15	OA15	A15
*RA16	OA16	A16
--	OA17	A17
--	OA18	A18

* (Hi/Lo)

Revision History

2.30 17/06/2016 – Final version for PCB production
Deleted Address, Data & Control bus buffers
Added LTC690x for adjustable master clock option
Added Q1 to limit current draw from U12 for D2
Deleted ROM, RAM and I/O Decode GALs – now CPLD only
Slow clock (SQW from RTC) selected by link position
Renamed all jumpers for consistency
Deleted MAX705 – RESET circuit moved to backplane PCB
Deleted bulk power capacitor – moved to backplane PCB
Deleted X2 – PHI4 generated in CPLD again
Deleted the serial divider (74xx193) – moved to CPLD
Deleted the clock divider (74xx193) – moved to CPLD
Deleted clock speed select switches

For development board revision history, see schemati versions prior to 2.30

Note 1 : Pin not available in the, otherwise compatible, 160 MCell EPM7160S

2.20 29/03/2016 – Added oscillator for PHI4 (as X2) (simpler than dividing PHI)
– Removed 48MHz test oscillator (X2) to make space for U13
– Moved U22 to common board (as U13), divide PHI/13 outside CPLD
2.19 12/03/2016 – RTC Mode changed to Intel (for I/O Wait logic on Video board)
–/RTCRW signal added to CPLD, replacing /WR on RTC
2.18 07/03/2016 – Deleted V2.16 mods (JP8 and /VDPWR bus signal)
2.17 29/02/2016 – Added R14, pull up on CPLD WAIT input
2.16 21/02/2016 – Video timing mods, added JP8 to disconnect CPU WAIT from bus
Added new /VDPWR signal to bus on Pin C21
2.15 20/02/2016 – CPLD Optimisation : Fed PHI back into GCLK2 (Pin 2)
2.14 14/02/2016 – CPLD Optimisation :
BUSREQ and "Special Reset " deleted.
2.13 02/02/2016 – GAL CTC Division Removed
Re–purposed PS2 as ROM Hi/Lo select (mono/colour CP/M)
Added U12 (HC244) to CPLD board design to replace Control
GAL (U10). (GAL I/O disconnected, but still available for use)
Version 2.12 changes removed (C/T3 and ZC0) from CPLD again
2.12 29/01/2016 – Added CT/3 (O) and ZC0 (I) to CPLD for autosetting of CTC
counters based on CPU speed (courtesy of Tony Brewer)
2.11 25/02/2015 – Added U11 (HC273) to CPLD board design for Page Port outputs
to the bus (saves 7 CPLD I/O pins)
– Added 48 MHz oscillator (link selectable, for testing)
– Connected CTC C/T3 & ZC0 to U10 to support setting MTX ROM
timing interrupt frequency based on system clock speed
(courtesy of Tony Brewer)
–
2.10 24/01/2015 – Moved Data buffer to CPU output pins
– Added U10 : Z80 Control ourput buffer & misc logic
– Tied RTC R/*W to /WR, removed from CPLD
2.09 06/01/2015 – Moved Address buffers to CPU output pins
2.08 04/01/2015 – Combined ROM/RAM address lines for CPLD option
2.07 07/12/2014 – Added JP5 – CPLD Diag output destination select :
– To CPU DEBUG LED, or
– To Diag board display latch option 4 (via backplane)
– Tied RTC /CS to 0V, removed from CPLD
2.06 25/11/2014 – Added JP4 for CPU Reset Selection (Normal / Special)
Added JP3 for RTC Bus Mode Selecton
Moved CPLD /RESET input to Pin 1
Added /CPU_RESET output to Pin 60
Added RFSH input to Pin 2
Added weak pull–ups (10K) to data bus
Modified CPLD RAM/ROM Select
Deleted on–board I/O connector
2.05 21/11/2014 – Removed CTC clock inverters, deleted signals from CPLD
(Not required for CMOS CTC, freeing up CPLD I/O)
Connected CTC Serial clocks direct to backplane
2.04 15/11/2014 – Corrected orientation of Page Port Flip–Flop, U23
Changed CTC to use PHI instead of PHI4
2.03 04/11/2014 – Added link to allow disable of RESET to RTC chip
Swapped positions of R2&R0 on CPLD ("as–built")
2.02 19/10/2014 – Split schematic to include PLD and CPLD options
2.01 19/10/2014 – Moved the CPU & CTC clocks into the CPLD
Moved the serial clock inverters into the CPLD
Removed clock pull ups

2.00 10/10/2014 – MTXPlus+ Design
1.00 --------- – Draft based on MTX 4000–04 computer board

Sheet: /CPU Sheet 2/
File: CPU_Sheet2.sch

Title: MTXPlus+ CPU Board –

Size: A3	Date: 2016–04–02	**Rev: 2.30**
KiCad E.D.A. kicad 4.0.1–stable		Id: 2/2