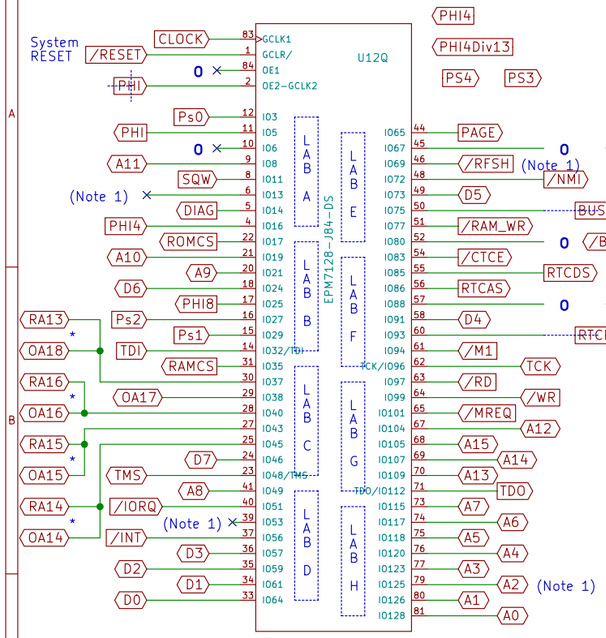
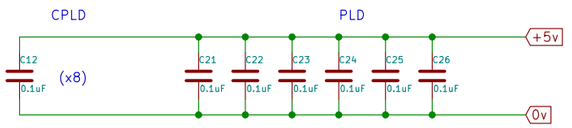
X1
TCXO3
+5V
GND 32 MHz NC
FREQ
Osc Select
JP8
CLOCK
X2
TCXO3
GND 4 MHz NC
PHI4
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13
0.1uF
D1
LED
R8
220R
/VDPINT
Temporary
For CPU Timing
Tests
C/T0
/M1
JP7
C/T3
ZC0
5v
R14 4.7K
R3 R4 R5 R6 1K
JP8
/WAIT
/INT
/NMI
/BUSRQ
/BUSAK
U1
WAIT
INT
NMI
BUSRQ
BUSAK
/M1_in
/MREQ_in
/IORQ_in
/WR_in
/RD_in
M1
MREQ
IORQ
WR
RD
/RFSH_in
/HALT_in
REFSH
HALT
RESET
CLK
Z80-CPU
PHI
/RESET
(Deleted)
CPU Reset Select
JP2
RP1 10K
U2
CLK/TRG3
CLK/TRG1
CLK/TRG2
CLK/TRG0
IEI
CLK
RESET
RD
IORQ
M1
CE
CS0
CS1
ZC/TO0
ZC/TO1
ZC/TO2
IEO
INT
D0 D1 D2 D3 D4 D5 D6 D7
Z80-CTC_DS
C/T3
CK4/13
C/T0
+5v
4K7
R7
PHI
/RESET
/RD
/IORQ
/M1
/CTCE
A0
A1
ZC0
SER01
SER02
/IEO
/INT
U6
U7
U8
74HC245
/BUSAK
A->B
CE
BUFFER BYPASSED
Select
JP6
(Spare)
GAL22V10
IO/CK I0 I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11
IO9 IO8 IO7 IO6 IO5 IO4 IO3 IO2 IO1 IO0
VCC GND
U10
Serial Divider
74HC193
PHI4
UpDw
UpUp
TcUp
P0 P1 P2 P3
Mr
TcDw
PL
Q0 Q1 Q2 Q3
U13
CK4/13
U12
74LS244
2A1 2A2 2A3 2A4 1A4 1A3 1A2 1A1
2Y1 2Y2 2Y3 2Y4 1Y4 1Y3 1Y2 1Y1
1G 2G
Page Port
74HC273
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
U11
Cp
Mr
PAGE
P0 P2 R0 R2 /RELCPMH R1 P3 P1
U3
SRAM_512K0
OA14 OA15 OA16 OA17 OA18
/RAM_WR
RAMCS
U4
CP/M ROM
(Colour
or Mono)
27C010
RA13 RA14 RA15 RA16
PGM
VPP
ROMCS
(Spare)
JP1
Intel
(Default)
(Optional)
Motorola
Bus Select
JP4
DS12887
MOT
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
SQW
IRQ
RESET
DS
R/W
AS
CS
Vcc
GND
RTCDS
/RTCRW
RTCAS
10K R9
JP3
LINK
(Default)
(Open)
SW1
RESET
U9
MAX705
MR
VCC
GND
PFI
WDO
RESET
WDI
PFO
100K R15
RP2
10K
PWR_FLAG
VSS GND VDD VCC
Top Plane
LK-P1
LK-P2
J0
C96ABC_MTXP
Default
0v
Default
+5v
Default
+3.3v
LK-P3
LK-P4
Bottom Plane
Sheet: /
File: CPU_Ver2_221.sch
Title: MTXPlus+ CPU Board –
Size: A3
Date: 2016-04-02
KiCad E.D.A. kicad 4.0.1-stable
Rev: 2.21
Id: 1/2
Sheet: CPU_Sheet2_220
File: CPU_Sheet2_220.sch



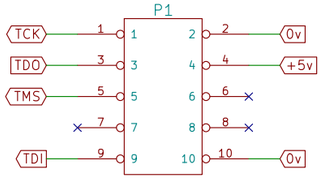
NOT CONNECTED	OPTIONAL	REQUIRED
~~(/BUSRQ)~~	/WR ✓	/M1 ✓
	/HALT ✓	/RD ✓
	/NMI ✓	/MREQ ✓
	/RFSH ✓	/IORQ ✓
	/WAIT ✓	/RESET ✓
		/INT ✓
		A12 ✓
		A11 ✓
		A10 ✓
		A9 ✓
		A8 ✓
		~~BUSAK~~ ✓
		/BUSAK ✓
		~~/DATADIR~~ ✓

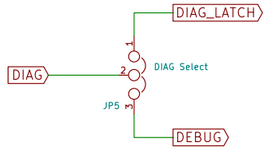


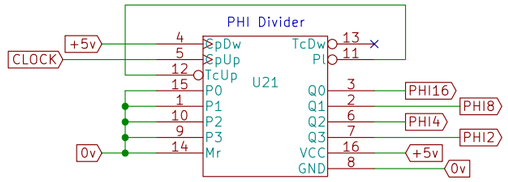
MEMORY ADDRESS DECODING (v2.13)

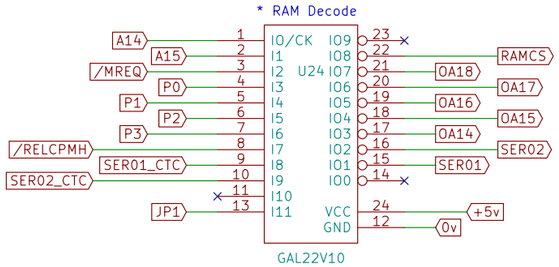
EPM7128S ROM	EPM7128S RAM	GALxxVyy PIN	GALxxVyy RAM	GALxxVyy ROM
OA18	n/a	A13	n/a	RA13
OA14	OA14	A14	OA14	RA14
OA15	OA15	A15	OA15	RA15
OA16	OA16	A16	OA16	--
--	OA17	A17	OA17	--
--	OA18	A18	OA18	--

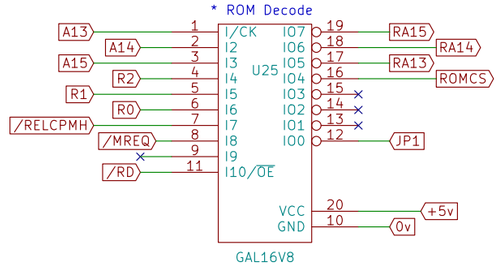
* For details, see the website

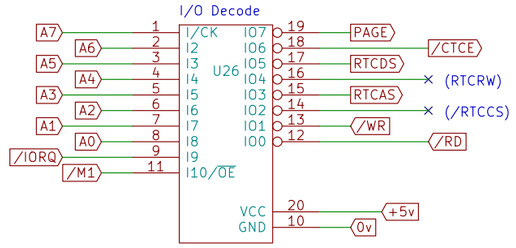


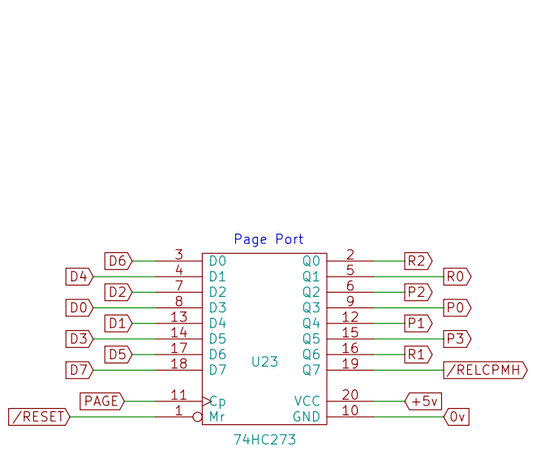


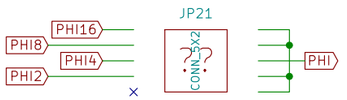




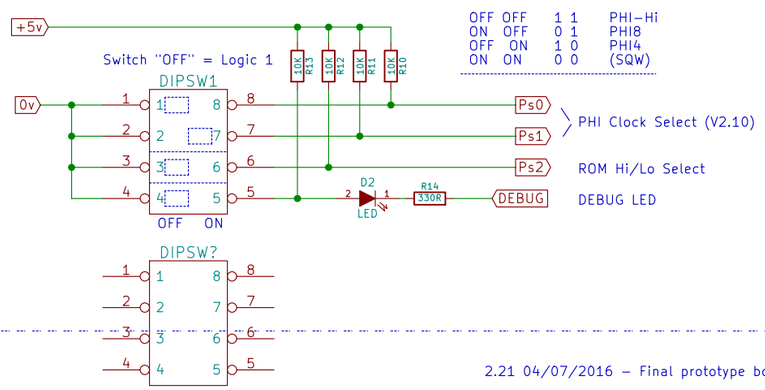








Switch 1	Switch 2	Logic 1	Logic 0	Clock
OFF	OFF	1	1	PHI-Hi
ON	OFF	0	1	PHI8
OFF	ON	1	0	PHI4
ON	ON	0	0	(SQW)



2.21 04/07/2016 – Final prototype board before PCB manufacture

Note 1 : Pin not available in the, otherwise compatible, 160 MCell EPM7160S

Revision History

2.20 29/03/2016 – Added oscillator for PHI4 (as X2) (simpler than dividing PHI)
– Removed 48MHz test oscillator (X2) to make space for U13
– Moved U22 to common board (as U13), divide PHI/13 outside CPLD
2.19 12/03/2016 – RTC Mode changed to Intel (for I/O Wait logic on Video board)
–/RTCRW signal added to CPLD, replacing /WR on RTC
2.18 07/03/2016 – Deleted V2.16 mods (JP8 and /VDPWR bus signal)
2.17 29/02/2016 – Added R14, pull up on CPLD WAIT input
2.16 21/02/2016 – Video timing mods, added JP8 to disconnect CPU WAIT from bus
Added new /VDPWR signal to bus on Pin C21
2.15 20/02/2016 – CPLD Optimisation : Fed PHI back into GCLK2 (Pin 2)
2.14 14/02/2016 – CPLD Optimisation :
BUSREQ and "Special Reset " deleted.
2.13 02/02/2016 – GAL CTC Division Removed
Re-purposed PS2 as ROM Hi/Lo select (mono/colour CP/M)
Added U12 (HC244) to CPLD board design to replace Control GAL (U10). (GAL I/O disconnected, but still available for use)
Version 2.12 changes removed (C/T3 and ZC0) from CPLD again
2.12 29/01/2016 – Added CT/3 (O) and ZC0 (I) to CPLD for autosetting of CTC counters based on CPU speed (courtesy of Tony Brewer)
2.11 25/02/2015 – Added U11 (HC273) to CPLD board design for Page Port outputs to the bus (saves 7 CPLD I/O pins)
– Added 48 MHz oscillator (link selectable, for testing)
– Connected CTC C/T3 & ZC0 to U10 to support setting MTX ROM timing interrupt frequency based on system clock speed (courtesy of Tony Brewer)
–
2.10 24/01/2015 – Moved Data buffer to CPU output pins
– Added U10 : Z80 Control ourput buffer & misc logic
– Tied RTC R/*W to /WR, removed from CPLD
2.09 06/01/2015 – Moved Address buffers to CPU output pins
2.08 04/01/2015 – Combined ROM/RAM address lines for CPLD option
2.07 07/12/2014 – Added JP5 – CPLD Diag output destination select :
– To CPU DEBUG LED, or
– To Diag board display latch option 4 (via backplane)
– Tied RTC /CS to 0V, removed from CPLD
2.06 25/11/2014 – Added JP4 for CPU Reset Selection (Normal / Special)
Added JP3 for RTC Bus Mode Selecton
Moved CPLD /RESET input to Pin 1
Added /CPU_RESET output to Pin 60
Added RFSH input to Pin 2
Added weak pull-ups (10K) to data bus
Modified CPLD RAM/ROM Select
Deleted on-board I/O connector
2.05 21/11/2014 – Removed CTC clock inverters, deleted signals from CPLD
(Not required for CMOS CTC, freeing up CPLD I/O)
Connected CTC Serial clocks direct to backplane
2.04 15/11/2014 – Corrected orientation of Page Port Flip-Flop, U23
Changed CTC to use PHI instead of PHI4
2.03 04/11/2014 – Added link to allow disable of RESET to RTC chip
Swapped positions of R2&R0 on CPLD ("as-built")
2.02 19/10/2014 – Split schematic to include PLD and CPLD options
2.01 19/10/2014 – Moved the CPU & CTC clocks into the CPLD
Moved the serial clock inverters into the CPLD
Removed clock pull ups
2.00 10/10/2014 – MTXPlus+ Design
1.00 -------- – Draft based on MTX 4000-04 computer board

Sheet: /CPU_Sheet2_220/
File: CPU_Sheet2_220.sch

Title: MTXPlus+ CPU Board –

Size: A3	Date: 2016-04-02	**Rev: 2.21**
KiCad E.D.A. kicad 4.0.1-stable		Id: 2/2