MTX Rom Board

Model Jumper

(MTX512)

(MTX500)

(RS128)

RomD

74HC32 OR x4

0v			3y	RomCS
2*MEMRD	2y		3a	(RomD)
*RD	2b		3b	(Rom7)
*mreq	2a		4y	IORW
*MEMWR	1y		4a	*iorq
*WR	1b		4b	*wr
*mreq	1a		5v	

bottom

512k x 8bit FLASH ROM

0V		D3	
D2		D4	
D1		D5	
D0		D6	
A0		D7	
A1		*CE	RomCS
A2		A10	
A3		*OE	*MEMRD
A4		A11	
A5		A9	
A6		A8	
A7		A13	Q0
A12		A14	Q1
Q2	A15	A17	Q4
Q3	A16	*WE	5V
Q5	A18		5v

0v	ser 2
ser 1	*re/cpm
r2	r1
r0	p3
p2	p1
p0	lnk12
*int	*nmi
*busreq	*wait
*busak	*halt
*rfsh	PHI
*mi	*wr
*rd	*iorq
*mreq	*reset
0v	0v
-v	12v
5v	5v
D7	d6
D5	d4
D3	d2
D1	d0
A15	a14
A13	a12
A11	a10
A9	a8
A7	a6
Keyway	Keyway
0v	A5
A4	A3
A2	A1
A0	*GROM

74HC138 3 to 8

0V		Y6	
Y7		Y5	
A14	G1	Y4	
A15	*G2B	Y3	rs128
P3	*G2A	Y2	
P2	C	Y1	mrx512
P1	B	Y0	mtx50
P0	A	5v	

74HC138 3 to 8

0V		Y6	
(rom7)	Y7	Y5	
A13	G1	Y4	
A14	*G2B	Y3	
A15	*G2A	Y2	
R2	C	Y1	
R1	B	Y0	
R0	A	5v	

74HC273 D type flip flop

0v		cp	(page)
Q3		Q4	
D3		D4	
D2		D5	
Q2		Q5	
Q1		Q6	nc
D1		D6	
D0		D7	
Q0		Q7	nc
(reset)	mr	5v	

74HC20 Q NAND X2

0v			2Y	FFH
FFL	1Y		2A	A7
A3	1D		2B	A6
A2	1C		NC	
NC			2C	A5
A1	1B		2D	A4
A0	1A		5v	

74HC138 3 to 8

0V		Y6	
Y7		Y5	
5v	G1	Y4	
(FFL)	*G2B	Y3	
(FFH)	*G2A	Y2	
0v	C	Y1	
0v	B	Y0	page
(IOWR)	A	5v	

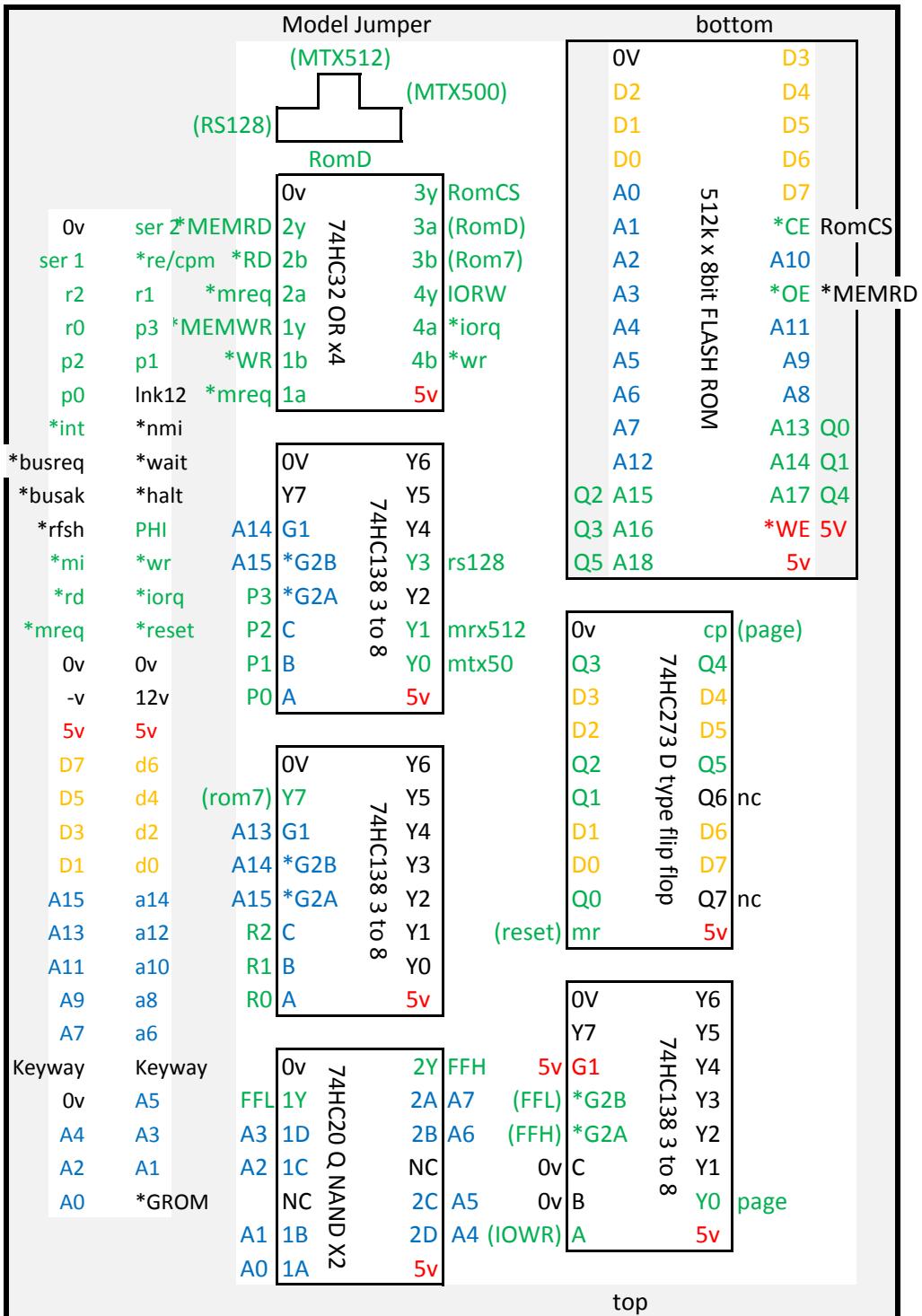top

ROM does 2 jobs

Paged in as ROM 7 it's the controlling foftware
Paged in bank 1 of the half ram page, it's the game data store

Paging for rom 7 - R15=0 R14=0 R13=1 R0=1 R1=1 R2=1
Paging for Bank1 R15=0 R14=1 P2=0 P3=0 P0/P1=0,1 or 3 for MTX500/MTX512/RS128
Ouput port selected when IOWR low(via OR) and A0-A7 all high(via nand)

LS138 inputs 2 low one high CS, and 3 selectors