

BILL OF MATERIALS

C1	1uF	IC1	74LS273	Q1	BC107
C2	22uF	IC2	74LS244	R1	10K
DC1	47nF	IC3	74LS74	R2	10K
DC2	47nF	IC4	WD1793	R3	4K7
DC3	47nF	IC6	74LS123	R4	4K7
DC4	47nF	IC7	2764	R5	4K7
DC5	47nF	IC8	74LS06	R6	4K7
DC6	47nF	IC9	74LS06	R7	220
DC7	47nF	IC10	PAL14L4	R8	220
DC8	47nF	IC11	PAL14L4	R9	220
DC9	47nF			R10	220
DC10	47nF			R11	330
D1	1N4148	4-Bit DIP Switches		R12	330
D2	1N4148	SW1-1	SW2-1	R13	330
D3	1N4148	SW1-2	SW2-2	R14	330
D4	1N4148	SW1-3	SW2-3	R15	220
D5	1N4148	SW1-4	SW2-4	R16	220
D6	1N4148			R17	100K
D7	1N4148			R18	50K
D8	1N4148			R19	1K
J0	MTX500/512 Edge Connector				
J2	Floppy Drive Data Connector				
J3	External +5V Input				

PAL LOGIC EQUATIONS

IC10
 /MOTOR = /HLD * /MOTOR ON
 /CTLWR = /WR * /A7 * /A6 * /A5 * A4 * /A3 * A2 * /A1 * /A0 * M1 * /IORQ
 /CTLRD = /RD * /A7 * /A6 * /A5 * A4 * /A3 * A2 * /A1 * /A0 * M1 * /IORQ
 /FDCS = /A7 * /A6 * /A5 * A4 * /A3 * /A2 * M1 * /IORQIC10

DESCRIPTION
 MOTOR = HLD OR MOTOR ON
 CTLWR low for OUT 14H
 CTLRD low for IN 14H
 FDCS low for IN/OUT 10-13H

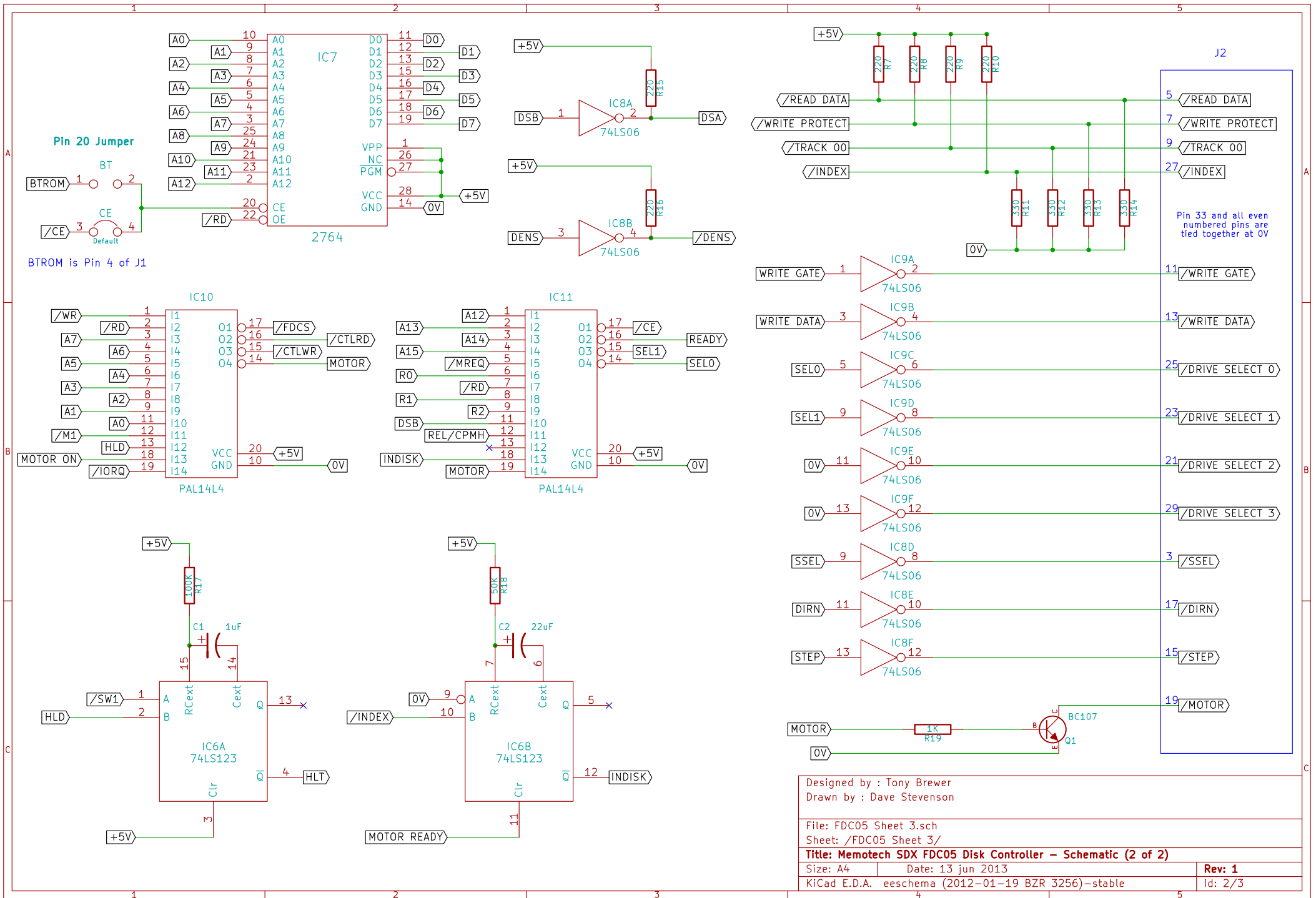
IC11
 /SEL0 = DSB + /MOTOR
 /SEL1 = /DSB + /MOTOR
 /READY = /INDISK + /MOTOR
 /CE = A13 * /A14 * /A15 * /MREQ * R0 * R1 * /R2 * /RELCPMH

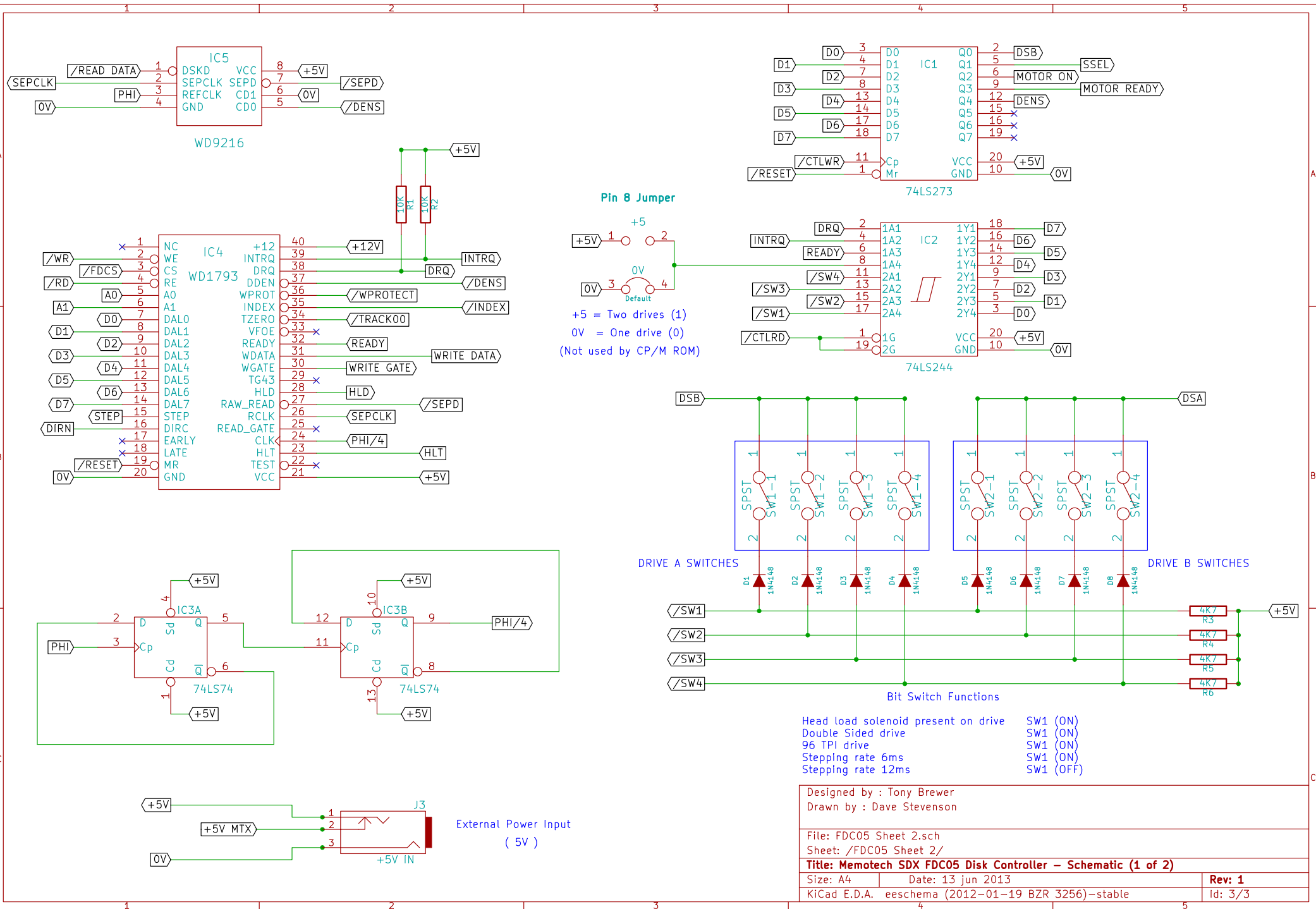
DESCRIPTION
 SEL0 = /DSB AND MOTOR = DSA AND MOTOR
 SEL1 = DSB AND MOTOR
 READY = INDISK AND MOTOR
 /CE low if RELCPMH low, MREQ low, ROM page 3, address 2000-3FFFH

Designed by : Tony Brewer
 Drawn by : Dave Stevenson

Sheet: FDC05 Sheet 2
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Sheet: FDC05 Sheet 3
 File: FDC05 Sheet 3.sch





Pin 8 Jumper

+5 1 2
0V 3 4
Default

+5 = Two drives (1)
0V = One drive (0)
(Not used by CP/M ROM)

Head load solenoid present on drive SW1 (ON)
 Double Sided drive SW1 (ON)
 96 TPI drive SW1 (ON)
 Stepping rate 6ms SW1 (ON)
 Stepping rate 12ms SW1 (OFF)

Designed by : Tony Brewer		
Drawn by : Dave Stevenson		
File: FDC05 Sheet 2.sch		
Sheet: /FDC05 Sheet 2/		
Title: Memotech SDX FDC05 Disk Controller - Schematic (1 of 2)		
Size: A4	Date: 13 jun 2013	Rev: 1
KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable		Id: 3/3