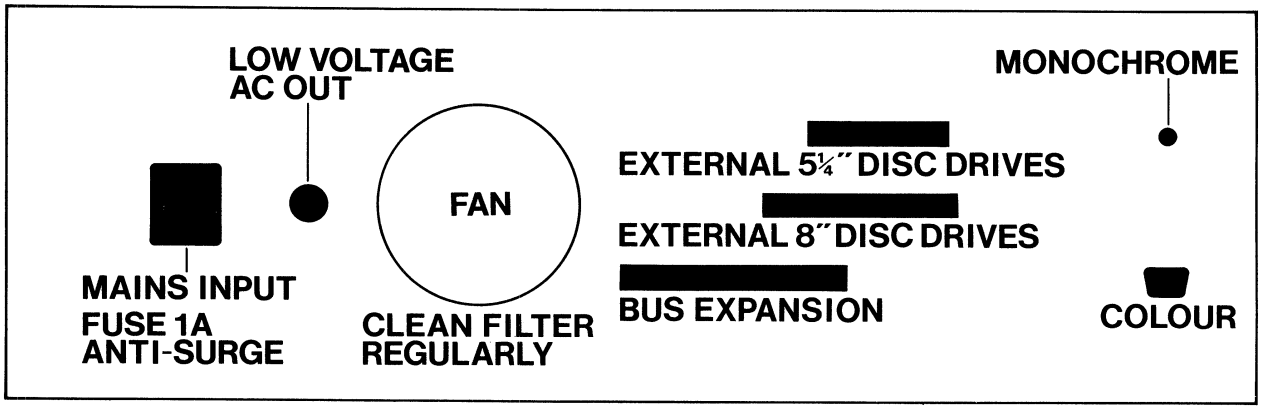
TECHNICAL MANUAL

MEMOTECH FLOPPY DISC SYSTEM TECHNICAL MANUAL

CONTENTS

Chapter One: MTX-FDX Overview



Rear Panel:

The rear panel of the MTX-FDX is shown above, From left to right it contains the following:-

1 A.C. Mains input socket (Fused 1A/S)

2 MTX low A.C. source

3 Fan & Filter. Clean filter regularly.

4 Bus expansion. Aperture for 60 way Bus expansion plug.

5 External 8" Disc Drive. Aperture for external 8" disc drive plug.

6 External 5¼" Disc drive. Aperture for external 5¼" disc drive plug.

7 Monochrome video output

8 Colour video output. The wiring diagram for the 9 way 'D' type can be seen in the 80 column card section.

Software Notes

MTX CP/M

The table below shows how the CP/M operating system and bootstrap code is stored on disc and located in memory. Note that the first two LOGICAL tracks of the disc are used for this purpose regardless of its physical structure. A logical track contains 26 LOGICAL sectors, and a logical sector contains 128 Bytes.

Track/Sector	Description	Located at:
0/1	COLD START LOADER etc.	100h ... 17FH
0/2 ... 0/17	CCP code (2KB)	SIZE-1D00 ... SIZE-1501
0/18 ... 1/19	BDOS code (3.5KB)	SIZE-1500 ... SIZE-701
1/20 ... 1/26	BIOS code (0.75KB)	SIZE-700 ... SIZE-401
	Unitiatlised temp. storage ie DIRBF, CHK, ALV	SIZE-400 ... (FREE-SPACE)

* SIZE is calculated from the CP/M system size. For example a 60K system has a SIZE value of 0F000h

Logical Tracks and Sectors

All track and sector level disc transactions (usually initiated by BDOS) are handled by CP/M's BIOS code. In the CP/M implementation BIOS simply relays disc access requests (read sector and write sector) to the dedicated disc handler software DISC.03 resident in high memory. DISC.03 accepts read and write requests to logical sectors 1..26 on logcial tracks 0..65535. CP/M is made to see all discs as having 26×128 byte sectors per track on as many tracks as necessary to make up the appropriate disc storage capacity. It is the job of DISC.03 to map these logical sector requests onto the physical storage device. This involves converting not only from 26 s.p.t. to N s.p.t. but also possibly from 256 bytes per sector to 128 bytes per access via a suitable de-blocking algorithm. In addition, CP/M disc parameter blocks are supplied by DISC.03 from an internal library containing one DPB for each of the configuration codes it supports. The DPBs are written in such a way that CP/M perceives all discs as having 26 sectors per track and 128 bytes per sector – differing amounts of storage capacity are accommodated by adjusting the number of logical tracks that CP/M sees.

The I/O Byte

Listed below are the physical interfaces/devices available on the MTX-FDX System. These have been given the mnemonics indicated for the sake of future references.

SIOA	Serial port A	IN/OUT
SIOB	Serial port B	IN/OUT
KBD	Ascii Keyboard	IN only
CTX	Centronics printer	OUT only
VDU	Visual display	OUT only

In addition to the above a user patchable jump table (referred to as the reflection table) is provided in low memory which may be used for passing control to user-installed custom device drivers. The table has 9 entries named RF0..RF8 and is located from 15hex onwards; at cold boot time it is initialised with the vectors indicated.

RF0	0015	CRTRDY – initialised to TTY
RF1	0018	PTRRDY – initialised to TTY
RF2	001B	LPTRDY – initialised to CTX
RF3	001E	CRTOUT – initialised to TTY
RF4	0021	PTPOUT – initialised to TTY
RF5	0024	LPTOUT – initialised to CTX
RF6	0027	CRTIN – initialised to TTY
RF7	002A	PTRIN – initialised to TTY
RF8	002D	CRTOUTPUT READY – initialised to TTY

The table below gives the relationship between CP/M's logical devices and the physical devices of the MTX-FDX.

		INPUT	**STATUS**	**OUTPUT**	**O/P STATUS**
CON:	field				
00	TTY:	KBD	KBD	VDU	—
01	CRT:	RF6	RF0	RF3	—
10	BAT:	RDR:	RDR:	LST:	—
11	UC1:	SIOB	SIOB	SIOB	—
PUN:	field				
00	TTY:	—	—	VDU	—
01	PTP:	—	—	RF4	—
10	UP1:	—	—	SIOA	—
11	UP2:	—	—	SIOB	—
RDR:	field				
00	TTY:	KBD	KBD	—	—
01	PTR:	RF7	RF1	—	—
10	UR1:	SIOA	SIOA	—	—
11	UR2:	SIOB	SIOB	—	—

		INPUT	STATUS	OUTPUT	O/P STATUS
LST:	field				
00	TTY:	——	——	VDU	NUL
01	CRT:	——	——	RF3	RF8
10	LPT:	——	——	CTXviaRF5	CTXviaRF2
11	UL1:	——	——	SIOB	SIOB

The Bootstrap Prom – 8K Versions

The 8KB bootstrap prom on the MTX-FDX Interface Card contains three software units: A bootstrap monitor program, ZMON.ASM, the VDU device driver, CRT.ASM and the Disc controller handler, DISC. The disc controller handler code is dependent on the particular controller board used in the system and thus determines its version number. At power up and reset time the prom is mapped-in in place of RAM from location 0 through to 7FFFh – leaving room for up to 32K bytes of prom. It subsequently gets control of the processor and loads itself into high RAM from 0F000h to 0FFFFh. Control is then passed to the newly initialised location 0F000h, at this point the prom is windowed out of the memory map and the Bootstrap Monitor Program signs on from RAM. After a system setup and RAM check sequence, provided no CR characters have been typed at the KBD, up to 10 attempts are made at booting, if all fail then the processor is halted. If a CR is typed during the ram check then the bootstrap monitor will enter its interactive mini-monitor mode and prompt the use for a command. The following commands are recognised:

S<addr> Substitute memory starting at address addr. Enter spaces to skip over locations without altering them, or any valid hex digit to change the value in ram, LF causes a skip to the next block of 16 locations, CR exits the command.

R Read hex file from SIOB at 9600 baud. Used to down-line-load programs via the serial port.

D Dialogue – the computer becomes a dumb terminal device, characters entered at KBD are sent to SIOB, characters received by SIOB are sent to the display. Terminate the command by typing ^Q.

B<dnn> The boot command may be used without parameters to simulate a power-on boot sequence. If parameters are given then d is used as the physical drive number B..I, and nn as the type code for the drive.

G<addr> Begins execution at addr.

Bootstrap Prom Version 03

CONTROLLER: SM2 FDCX1
NUMBER OF DRIVES: up to 4
PROM SIZE: 8K bytes
CONFIG CODES SUPPORTED: 0,1,2,3,4,5,6,7,10,11,12,13
TOAM VALUE: 0F000h

Physical Disc Format Table

CONFIG CODE	DRIVE H/WARE	PHYSICAL FORMAT	INTERLEAVE
00	5" */S,*/T	16 × 128B S/D s.p.t. 40Tk	1—2—3—4
01	5" D/S,*/T	16 × 128B S/D s.p.t. S0,S1	1—2—3—4
02	5" */S,*/T	16 × 256B D/D s.p.t. 40Tk	1—2—3—4
03	5" D/S,*/T	16 × 256B D/D s.p.t. S0,S1	1—2—3—4
04	5" */S,D/T	16 × 128B S/D s.p.t. 80Tk	1—2—3—4
05	5" D/S,D/T	16 × 128B S/D s.p.t. S0,S1	1—2—3—4
06	5" */S,D/T	16 × 256B D/D s.p.t. 80Tk	1—2—3—4
07	5" D/S,D/T	16 × 256B D/D s.p.t. S0,S1	1—2—3—4
10	8" */S	IBM 3740 26 × 128B S/D sectors-per-track 77Tk	1—2—3 Tk0,1 1——7 Tk2..76
11	8" D/S only	IBM 3740 both sides 77Tk	1—2—3—4
12	8" */S	IBM System 34 26 × 128B S/D Tk0, 26 × 256B D/D Tk1..76	1—2—3—4
13	8" D/S only	IBM 34 26 × 128 S/D Tk0,S0 26 × 256 D/D all other Tks	1—2—3—4
* *	*/S */T	means double or single sided means double or single track density	

Special Notes

Follow the controller manual when installing extra drives. In particular: set the DIL switches to the appropriate values on the controller board, install the correct link options on the drives and ensure that the drives at the physical end of the daisy chains are properly terminated. The highest capacity drive MUST be the last physical drive in its respective chain in order that all the used conductors are terminated.

Entries in the page 0 memory map

Some extensions to the standard CP/M entries have been implemented; these are indicated by asterisks.

ADDR	DESCRIPTION
0000..0002	Jump to warm boot (CB10S +3)
0003	I/O Byte
0004	Current logged drive number (0..8)
0005..0007	Jump to BDOS for system calls
0008..0014	Not used

I/O Reflection Jump Table

0015..0017	CRT ready test vector*
0018..001A	PTR ready test vector*
001B..001D	LPT ready test vector*
001E..0020	CRT output handler vector*
0021..0023	PTP output handler vector*
0024..0026	LPT output handler vector*
0027..0029	CRT input handler vector*
002A..002C	PTR input handler vector*
002D..002F	CRT output ready test vector*
0030..0037	Interrupt £6 handler space (not used)
0038..003A	Interrupt £7 space, used by DDT
003B..003F	Reserved by Digital Research
0040..0041	FREE – Free space pointer*
0042..0043	Console Command string pointer*
0044	Boot drive pointer 1..8 eqiv B..1*
0045	Retry counter. After a disc access this location will contain a value between 0 & 10 indicating 0 = hard error to 9 = soft error with 10 = no error.
0046..0047	TOAM – Top-of-available-memory pointer.*
0048..004F	Reserved for software expansion.*
0050..005B	Reserved by DR
005C..007C	Default FCB
007D..007F	DFCB extension
0080..00FF	Tbuff

High Memory

Certain essential routines are located in high memory above the top of CP/M. These routines, which occupy the very top pages of memory right up to 0FFFFh, provide not only the low-level drivers for the disc, display and keyboard hardware but also the disc parameter blocks, for all the drive types supported, and any necessary sector interleave tables for use by CP/M. At the time when the code was loaded into RAM from PROM it would also have contained the bootstrap monitor program, but once CP/M is running and the monitor is no longer required it may be overlaid. At cold boot time a pointer is set up in Page zero which gives the address of the lowest byte required by these routines – the TOP-OF-AVAILABLE-MEMORY pointer or TOAM. The value of TOAM is dependent on the version number of the PROM, a typical value might be 0F000, and it determines the maximum bootable CP/M system size. An nnK version of MTX CP/M requires a minimum of (nn*1024-512) bytes, this figure, however, allows almost no room for CP/M's allocation and directory check vectors (which sit on top of BIOS) – these should not be allowed to exceed the TOAM value. When configuring disc drives into a system (using the CONFIG command) the user will be informed of the FREE-SPACE and TOAM pointer values (the FREE-SPACE value defines the highest address used by CP/M), from these it is possible to calculate the breathing space remaining for use by the ENTER command. Any user-installed options or drivers should be squeezed in below (TOAM) and above the max value of the FREE-SPACE pointer, this may require the lowering of your CP/M system size. If extra code is installed in high ram, be sure to update TOAM to point in front of it. The table below provides more detailed information on the structure of high memory code.

High Memory Map

LOCN	DESCRIPTION
(FREE)---	Top of CP/M = start of free ram space used for: allocations & check vectors when configuring extra drives and as character storage space for ENTER commands.
*****	Block reserved for user jumps into installed code
0F2FD..	JP1 of user-installable jump table.
0F2FA..	JP2
0F2F7..	JP3
0F2F4..	JP4
0F2F1..	JP5
(TOAM)---	Start of Disc and CRT handlers or start of user installed code.
*****	Rom initialised interface area.
0FFA0----	Skew table for type 10 drives (26 bytes)
0FFC0.....	Serial number (6 digit)
0FFD0..	KBD input
0FFD3..	VDU output
0FFD6..	KBD ready
0FFE7	TRUST
0FFE8	DRVRQ
0FFE9	CFGBYT
0FFEA.	TRKRQ
0FFEC.	SECRQ
0FFEE.	DMARQ
0FFF0..	CONFIGURE
0FFF3..	READ LOGICAL SECTOR (128 BYTE)
0FFF6..	WRITE LOGICAL SECTOR (128 BYTE)
0FFF9..	BLOCK READ (N in B reg)
0FFFC..	INITIALISE
0FFFF	VERSION NUMBER

NOTE: The FDX Keyboard scanning routine is loaded from F000h to F300h and the Silicon Disc Handler is loaded below this. These both adjust the value of TOAM, so that any user installed options must take these into account.

I/O Port Assignments on the MTX-FDX

This section describes the MTX Series Port Map

00h
INPUT
IN(0) is used to set the printer STROBE (active low) to LOW. The event of interrupt while STROBE is low it would be good practice to reset STROBE within an interrupt routine extending over a period of more than a few microseconds.

OUPUT
OUT(0),d defines memory page address. The bit map is as follows:

D0 = P0
D1 = P1
D2 = P2
D3 = P3
D4 = R0
D5 = R1
D6 = R2
D7 = RELCPMH

where the nibble P(i) defines the RAM page address, the 3 bit R(i) defines the ROM page address and bit 7 defines a ROM based system (D7 = 0) or a RAM based system (D7 = 1). The latch is reset to 0 on CPU reset.

01h
INPUT
IN(1),d VDP read (mode = 0) together with port 02 provides two contiguous read/write ports for the VDP. See documentation on the TMS9918 Series. Note Z80 CPU address line A1 is connected to mode input.

OUTPUT
OUT(1),d VDP write (mode = 0).

02h
INPUT
IN(2),d VDP read (mode = 1)

OUTPUT
OUT(2),d VDP write (mode = 1)

03h
INPUT
IN(3) This line is used as an output strobe into the sound generator. After data has been latched into the output port (6) data may be immediately strobed in using this line. A total of at least 32 clock cycles must have elapsed before additional data may be strobed in using IN(3).

OUTPUT
OUT(3),d This is the cassette output serial line. Valid data is placed on DO. This data bit is latched and appears on the cassette ouput (MIC) after attenuation (−20dB*VCC) and low pass filtering.

04h
INPUT
IN(4),d This is a nibble port for monitoring the status of the Centronics type parallel printer port.

D0 = BUSY active high handshake line
D1 = ERROR active low
D2 = PE paper empty active high
D3 = SLCT printer in selected state active high

OUTPUT
OUT(4),d Parallel 8 bit printer data. Valid data should be latched into this port. When status on IN(4) reads not BUSY and selected, then data should be strobed after a delay of approximately 1 microsecond using IN(0) to force STROBE low. After a further delay of approximately 1 microsecond STROBE should be forced high using IN(4).

05h

INPUT

IN(5),d This port is used to read the least significant 8 bits from the ten bit sense line of the 8×10 keyboard matrix.

OUTPUT

OUT(5),d This latched port provides the 8 drive lines of the 8×10 keyboard matrix.

06h

INPUT

IN(6),d This port is used to read in the two most significant sense lines (D0 and D1) of the 8×10 keyboard matrix. The two bit country code switch is read on D2 and D3.

OUTPUT

OUT(6),d This port is used to provide latched data for the sound generator which is subsequently strobed using IN(3).

07h

INPUT

IN(7),d This is the input port for the uncommitted parallel input output port (PIO). Data may be latched in for reading with an active low pulse on the enable line, designated INSTB.

OUTPUT

OUT(7),d This is the output port of the PIO. It is a latched output with tri-state output control using OTSTB.

08, 09, 0A, 0Bh

These are four contiguous read/write ports for the four channels of the Z80A CTC.

08	ch0	input-VDPINT	out-no connect
09	ch1	input-4MHz/13	out-DART ser clock 0
0A	ch2	input-4MHz/13	out-DART ser clock 1
0B	ch3	input-CSTTE edge	out-none

0C, 0D, 0E, 0Fh

These are four contiguous read/write ports for the DART.

0C	chA	data
0D	chB	data
0E	chA	control
0F	chB	control

Ports 10h to 1Eh are currently unused with 1Fh reserved for cassette remote control.

Bit Level Port Descriptions

PORT 38..39 See Motorola 6845 Technical manual

PORT 30 WRITE

D0..D7 Correspond to A0..A7
Writing to this port initiates a VDU memory access.

PORT 31 WRITE

D0..D2	Correspond to A8..A10
D3..D4	Not used
D5	Write enable attribute memory
D6	Write enable ascii memory
D7	Write cycle when high/read when low

PORT 32 READ/WRITE

D0..D7 ALPHA or GRAPHIC character code bits 0..7

PORT 33 READ/WRITE (Attribute byte)

	MONOCHROME DISPLAY	COLOUR DISPLAY
D0	Underline	Red foreground
D1	No effect	Green foreground
D2	Bright-up	Blue foreground
D3	No effect	Red background
D4	Reverse video	Green background
D5	Background	Blue background
D6	---------- Blink ----------	
D7	---------- Graphics mode ----------	

Chapter Two: MTX-FDCX1 Floppy Disc Controller

CAPABILITIES

The FDCX1 board is capable of controlling four floppy disc drives. These may be any mix of 5.25" or 8", single or double-sided, single or double-density, and 96 or 48 TPI. Two interface connectors are provided, J2 is a 50-way connector for use with Shugart compatible 8" drives and J3 is a 34-way connector for Shugart compatible 5.25" drives. The 60-way edge connector is compatible with the MTX computer board bus but may be used with virtually any Z80 based system capable of supporting DMA transfers.

OPTIONS

Four on-board 8-way DIL-switches are used to characterise the drive hardware.

Head-load solenoid present on drive	SW1 (ON)
Extra, (variable) write precomp required	SW2 (ON)
Write precomp required on ALL tracks	SW3 (ON)
Write precomp required on tracks > 43	SW4 (ON)
Double-sided drive	SW5 (ON)
96 TPI drive	SW6 (ON)

Stepping rate select:	SW7	&SW8
	---	---
3ms 8" or 6ms 5"	OFF	OFF
6ms 8" or 12ms 5"	OFF	ON
10ms 8" or 20ms 5"	ON	OFF
15ms 8" or 30ms 5"	ON	ON

Drive number 1 is configured with the switch pack at board location 9E, likewise drives 2,3 and 4 are setup from the switches at 9D, 9C and 8B respectively. Links L1..L5 are used to setup the base IO port address. They select A7..A3 respectively active HI (h) or LOW (1).

Monostable multivibrators are used to generate head-load and motor-start delays; the nominal values being 50ms and 800ms respectively. Appropriate write pre-compensation schemes may be selected using DIL switches 2,3 and 4. Write data is only precompensated in double density mode and may be enabled or disabled for all tracks or tracks > 43 if desired. The minimal amount of write pre-compensation may be extended by switching DIL-switch 2 ON – this causes extra precompensation to be invoked as determined by RV1 (turn clockwise for minimum extra pre-comp, anti-clockwise for maximum extra pre-comp.)

OPERATION

Determination of drive size (5.25" or 8") is achieved by detecting which interface connector (J3 or J2 resp.) goes active once the given drive has been selected. The board contains logic to detect the state of readyness of 5.25" drives and also to engage the drive motors on any 5.25" drives installed. The FDCX1 board makes use of DMA techniques to perform data transfers between the FD1791 controller chip and main memory, no intermediate buffers are used and no interrupts are generated. The board occupies 8 I/O port locations configurable by means of links L1..L5 to any 8-port boundary – the default base location is 40H. The tables below show how the 8 ports are used.

I0 Port Allocations

ADDR	READ		WRITE
BASE+0	STATUS REG	FD1791	COMMAND REG
BASE+1	----------	FD1791 TRACK REG	----------
BASE+2	----------	FD1791 SECTOR REG	----------
BASE+3	----------	FD1791 DATA REG	----------
BASE+4	STATUS BYTE		CONTROL BYTE
BASE+5	----------		DRV SEL CHNG
BASE+6	----------		DMA LOW BYTE
BASE+7	----------		DMA HI BYTE

Status and control byte formats

BIT	STATUS BYTE	CONTROL BYTE
0	Step rate R0 (DIL-8)	Drive select Addr0
1	Step rate R1 (DIL-7)	Drive select Addr1
2	96 TPI when HI (DIL-6)	Drive select enable
3	D/Sided when HI (DIL-5)	D/Density mode when HI
4	INT from 1791	5" Drive mode (1Mhz) HI
5	DRQ from 1791	DMA Enable when HI
6	READY from 5" interface	Disc WRITE when HI
7	READY from 8" interface	Side Select

DAISY CHAINS

The FDCX1 board supports two daisy chains – one from J2 for up to four 8" disc drives and one from J3 for up to four 5.25" disc drives. The total number of drives cannot be greater than 4, however, as each must have a unique one-of-four drive select strap. The combined length of both daisy chains must be less than 10 feet and each must be properly terminated. Proper termination requires that if double-sided drives are installed then the drive at the physical end of the chain should be double sided, this ensures that the side select line is terminated correctly.

SOFTWARE

The version 08 disc handler software has been written especially for the FDCX1 controller board. It allows for 12 possible drive configuration codes which range from 5.25" S/S, S/D, 40 Track drives through 5.25" D/S, D/D, 80 Track drives and on to 8" D/S, D/D, 77 Track drives. These are summarized in the table below. The FORMAT program is capable of initialising media with any of these config codes. (Note that the double density formats use 256 byte sectors).

As a compatibility feature 48 TPI config codes are supported on 96 TPI drives (this is achieved by double-stepping) and allows 96 TPI drive users to read 48 TPI discs. Eight inch single and double density formats have been made compatible with those generated by DTC and SMS winchester controllers, these are the IBM industry standard formats.

Physical Disc Format Table

CONFIG	DRIVE	PHYSICAL FORMAT	INTERLEAVE
00	5" */S,*/T	16 × 128B S/D s.p.t. 40Tk	1--2--3--4
01	5"D/S,*/T	16 × 128B S/D s.p.t. S0,S1	1--2--3--4
02	5" */S,*/T	16 × 256B D/D s.p.t. 40Tk	1--2--3--4
03	5" D/S,*/T	16 × 256B D/D s.p.t. S0,S1	1--2--3--4
04	5" */S,D/T	16 × 128B S/D s.p.t. 40Tk	1--2--3--4
05	5" D/S,D/T	16 × 128B S/D s.p.t. S0,S1	1--2--3--4
06	5" */S,D/T	16 × 256B D/D s.p.t. 40Tk	1--2--3--4
07	5" D/S,D/T	16 × 256B D/D s.p.t. S0,S1	1--2--3--4
10	8" */S	IBM 3740 26 × 128B S/D	1--2--3 Tk0,1
		sectors-per-track 77Tk	1---7 Tk2..76
11	8" D/S	IBM 3740	1--2--3--4
	only	both sides 77Tk	

CONFIG	DRIVE	PHYSICAL FORMAT	INTERLEAVE
12	8" */S	IBM System 34 26 × 128B S/D Tk0, 26 × 256B D/D Tk1..76	1--2--3--4
13	8" D/S only	IBM 34 26 × 128 S/D Tk0,S0 26 × 256 D/D all other Tks	1--2--3--4
* *	*/S	means double or single sided	
	*/T	means double or single track density	

THE DRIVES

All drives, 5.25" and 8" must be Shugart interface compatible. They should also have the user-selectable options and jumpers set as from the factory – on 8" drives these are as follows: T1,T3,T4,T5,T6,HL,A,B,X,Z all plugged with one of DS1, DS2, DS3 or DS4 plugged. T2,DS,NP,8,16,D,D1,D2,D4,DDS,C,Y,DC all open and RR,RI,R,I,S,WP all shorts. In addition, the drive's −5V power supply rail may be optionally set to direct, or regulated with the −5VDC / −7 to −16VDC link; this should be set appropriately.

THE CONNECTORS

Pin numbers for connectors J2 and J3 on the FDCX1 board are derived from their correspondence with conductors in the ribbon cable – conductor 1 is marked with a red stripe and makes contact with pin 1 on the connector. Unfortunately this scheme is not used by disc drive manufacturers who number pins from the opposite end. Don't worry about plugging the connectors in the wrong way round – no electrical harm will be done but any discs installed may have their data and format corrupted. Connectors J2 and J3 have alternate (even numbered) pins grounded, the table below gives designations for the remaining pins.

PIN	J2 – 8" INTERFACE	J3 – 5" INTERFACE
1	------	------
3	------	SIDE SEL
5	READ DATA	READ DATA
7	WRITE PROTECT	WRITE PROTECT
9	TRACK 00	TRACK 00
11	WRITE GATE	WRITE GATE
13	WRITE DATA	WRITE DATA
15	STEP	STEP
17	DIRECTION	DIRECTION
19	DRIVE SEL 4	RADIAL MOTOR ON
21	DRIVE SEL 3	DRIVE SEL 3
23	DRIVE SEL 2	DRIVE SEL 2
25	DRIVE SEL 1	DRIVE SEL 1
27	------	INDEX
28	READY	DRIVE SEL 4
31	INDEX	------
33	HEAD LOAD	HEAD LOAD
35	------	
37	SIDE SEL	
39	------	
41	------	
43	------	
45	------	
47	------	
49	LOW WRITE CURRENT	

J1 – Bus expansion connector

1	----	GND
2	Reserved	
3	Reserved	
4	Reserved	
5	<-->	A0
:	::::	:
:	::::	:
20	<-->	A15
21	Reserved	
22	Reserved	
23	Reserved	
24	----	+5v
25		
26	<-->	D0
:	::::	:
:	::::	:
33	<-->	D7
34	Reserved	
35	Reserved	
36	Reserved	
37	Reserved	
38	----	+5v
39	<---	RES
40	--->	MREQ
41	<---	IORQ
42	<-->	RD
43	<-->	WR
44	<---	M1
45		
46	<---	PHI – INVERTED
47	Reserved	
48	Reserved	
49	<---	BUSAK
50	<---	WAIT
51	--->	BUSRQ
52	Reserved	
53	Reserved	
54		KEY-WAY SLOT
55		
56		
57	Reserved	
58		
59	----	+12v
60	----	GND

Chapter Three: 80 Column Board

Visual Display Software (CRT.ASM) Control Code Definitions

The visual display system built into the 80 Column Board is a powerful and complex piece of hardware, and it therefore has a correspondingly complicated set of control codes to manipulate it, these are described below. A brief account of the visual display hardware will be given in order that the control code set can be related to it.

The display hardware contains 2K × 16 bit words of memory, each of the 1920 (80 × 24) character locations has one 16 bit data word associated with it. Two character generator proms are provided, one for ALPHA characters and one for the bit-mapped GRAPHICS characters. They each contain 256 shapes, one of which is addressed by the most significant byte of the character word. The least significant byte of the character word, referred to as the attribute byte, simply controls the way in which the character byte is displayed and amongst other things selects which character generator is used. In general each bit of the attribute byte has a particular and individual function associated with it, these are summarised in the table below.

The 256 entries in the ALPHA character generator prom are split up into 3 groups: the STANDARD character set of 96 symbols, the ALTERNATE set of 96 slightly different symbols and 64 special graphics symbols (independent of the bit-mapped graphics set). The ALPHA character generator regions are given below. The GRAPHICS character generator simply contains all the 256 possible combinations of the 8 pixels available in a graphics character.

The effects of the bits making-up the attribute byte are different depending on whether the display is being used with a colour or monochrome TV monitor – it controls either foreground and background colour or the various monochrome attributes such as under-line, bright-up, or reverse-video. Note that the attributes are NOT mutually exclusive and may be combined at will.

Effects of Bits in the Attribute Byte.

BIT	MONOCHROME DISPLAY		COLOUR DISPLAY
1	Underline		Red foreground
2	No effect		Green foreground
3	Bright-up		Blue foreground
4	No effect		Red background
5	Reverse video		Green background
6	Background		Blue background
7	----------	Blink	----------
8	----------	Graphics mode	----------

Effects of Bits in the ASCII Byte

CHARACTER GENERATOR REGIONS

DDDDDDDD 76543210		
000XXXXX	0.. 31	Special Graphics set (upper case equiv)
001XXXXX	32.. 63	Standard Alpha set (numerals)
010XXXXX	64.. 95	Standard Alpha set (upper case)
011XXXXX	96..127	Standard Alpha set (lower case)
100XXXXX	128..159	Special Graphics set (lower case equiv)
101XXXXX	160..191	Alternate Alpha set (numerals)
110XXXXX	192..223	Alternate Alpha set (upper case)
111XXXXX	224..255	Alternate Alpha set (lower case)

GRAPHICS CHARACTER CODE INTERPRETATION

D0..D7 represent the pixels of the graphics block:

b0	b1
b2	b3
b4	b5
b6	b7

CONTROL CODE SET

ASC	CNTL	NME	PERAMS	DESCRIPTION
0	@	NUL		null
1	A	DOT	x,y	Plot point at X,Y in (160 × 96)
2	B	VCT	x,y,x,y	Plot vector between the 2 co-ords
3	C	CXY	x,y	Position cursor to X,Y in (80 × 24)
4	D	BKG	n	Set background colour-attrib for printed and non-printed characters: n=0 to 7 corresponds to D3..D5 in the attribute byte specification
5	E	EOL		Erase to end of line
6	F	ATR	m	m=0..255 sets up the attrib bytes
7	G	BEL		Sounds the bell
8	H	BS		Back space, cursor left.
9	I	TAB		Tabulate to next block of 8 columns
10	J	LF		Line feed, cursor down
11	K	UP		Cursor up
12	L	CLR		Clear screen and home cursor
13	M	CR		Carriage return, cursor to LHS
14	N	BL		Blink-on
15	O	BLO		Blink-off
16	P	BLK	*	Black foreground
17	Q	RED	*	Red foreground
18	R	GRN	*	Green foreground
19	S	YEL	*	Yellow foreground
20	T	BLU	*	Blue foreground
21	U	MAG	*	Magenta foreground
22	V	CYN	*	Cyan foreground
23	W	WHT		White foreground
24	X	INI		Initialise to standard attrib config.
25	Y	FWD		Cursor forwards
26	Z	HME	ch..	Cursor to top LHS, home position
27	^(	ESC		Escape sequence, see next table
28	^/	SCR		Scroll mode
29	^)	PGE		Page mode or ROLL
30	^^	CON		Cursor ON
31	^	CSO		Cursor OFF

x,y	Are in offset binary. Add 32 to the required
m	X,Y co-ords
n	Must be specified in binary
*	May be binary or ascii

The effect of these codes when used on a monochrome display will correspond to setting the appropriate bits in the field D0..D2 of the attribute byte. NOTE: these codes affect printing characters only.

Printing characters are those which actually appear on the screen: Non-printing characters are generated by control codes such as CLR, EOL and ESC I, graphics plots and dots are also treated as non-printing characters. Non-printing characters may be given different attributes to the printing characters if desired.

ESCAPE SEQUENCE CODES

CHR	PARAM	DESCRIPTION
S		Use standard character font
A		Use alternate character font
G		Use special graphics font
C		Scroll mode
D		Page mode
E		Cursor on
F		Cursor off
X	ch	Simulate control character ch
I		Insert a blank line at cursor line, shifting the lines below down
J		Delete the current cursor line, shifting the lines below up
W	n	Set up the write mask:
	m	n=0 : allow ascii and attrib writes
	m	n=1 : allow only ascii writes
	m	n=2 : allow only attrib writes
T	n	Set printing character attrib byte to m (0..255)
U	n	Set non-printing attribute byte to m (0..255)
V	n	Set both attribute bytes to m (0..255)
P		Set bit n (1..8) of printing attrib byte *
N		Set bit n (1..8) of non-printing attrib byte *
B		Set bit n (1..8) of both attribute bytes *

n	May be in ascii or binary
m	Must be in binary
*	If n=0 then whole byte is reset

J8 – Video outputs

1	GND
2	Monochrome out
3	Mixed sync – strap to pin 2 for comp. vid.
4	H-Sync
5	V-Sync
6	key
7	RED
8	GREEN
9	BLUE
10	SYNC
11	+5v
12	GND
13	Speaker (−)
14	Speaker (+)
15	Lpen

Links

LS,LG,LR,LB

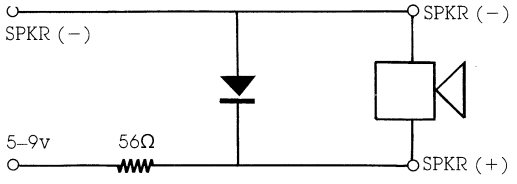
\+ active high signals on J8

− active low – default

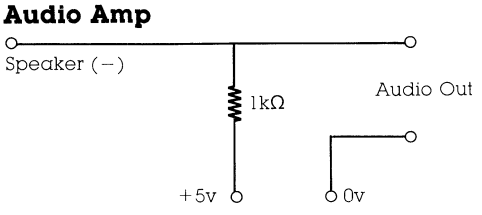
CONNECTIONS FOR 9 WAY 'D' TYPE: (Colour Video)

Pin			
1	Red	6	GND
2	Green	7	SY
3	Blue	8	Lpen i/p
4	HSY	9	Speaker (−)
5	VSY		Audio Out

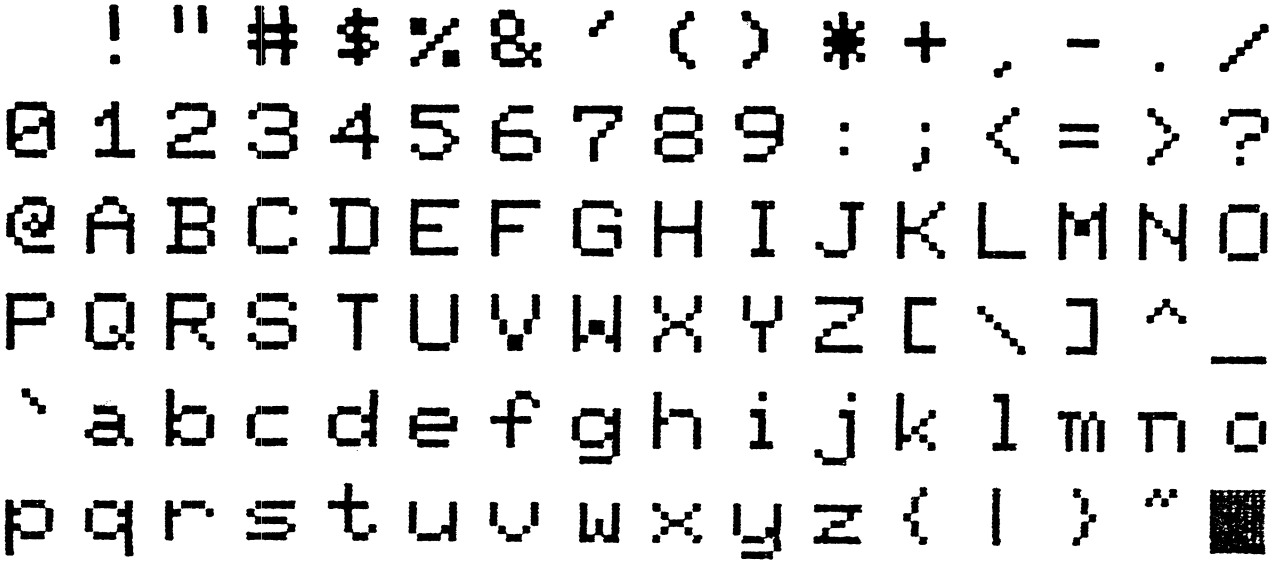
8 Ohm Speaker



Audio Amp



STANDARD CHARACTER SET

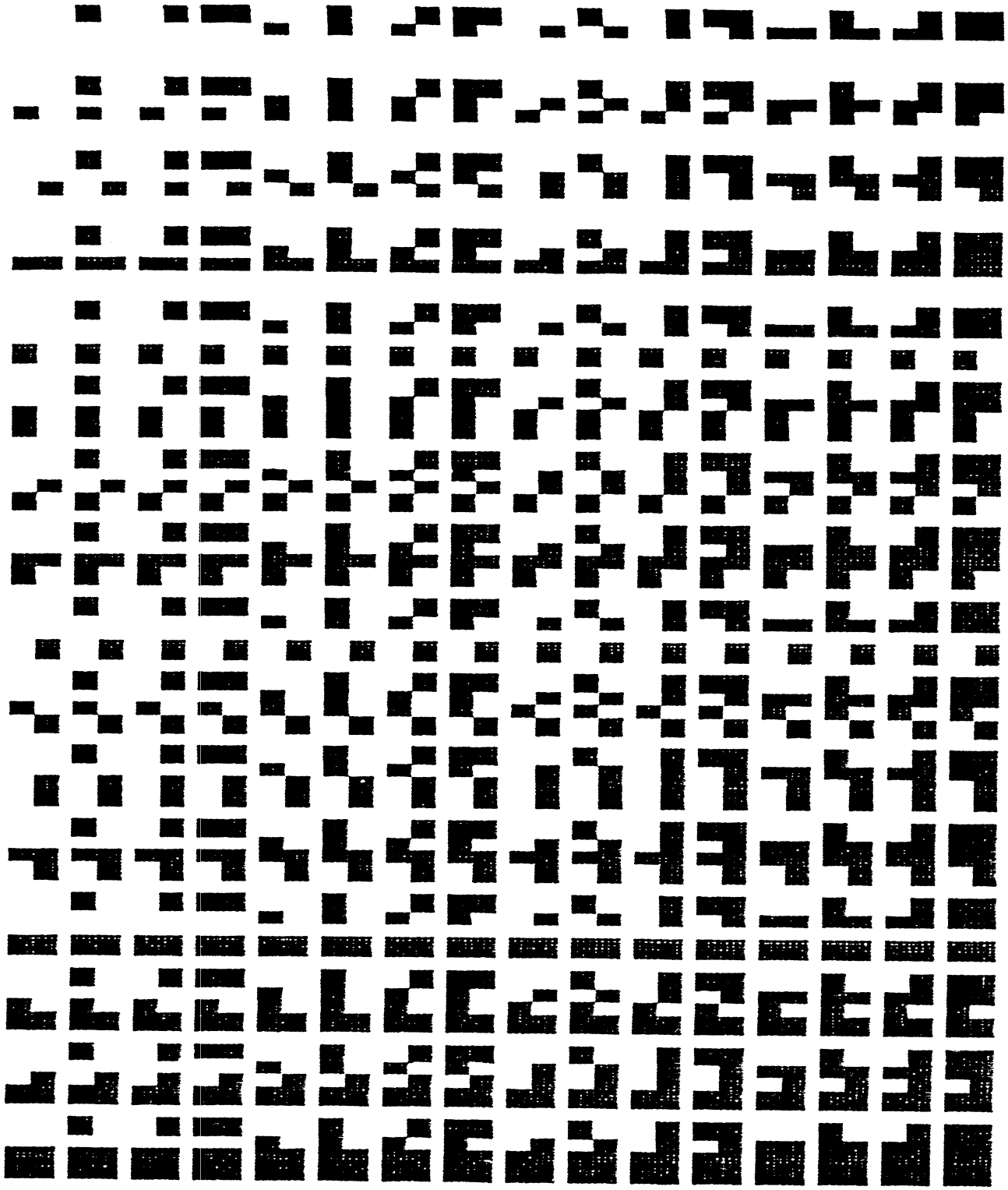


ALTERNATE CHARACTER SET

SPECIAL GRAPHICS SET

FULL ALPHA PROM SET

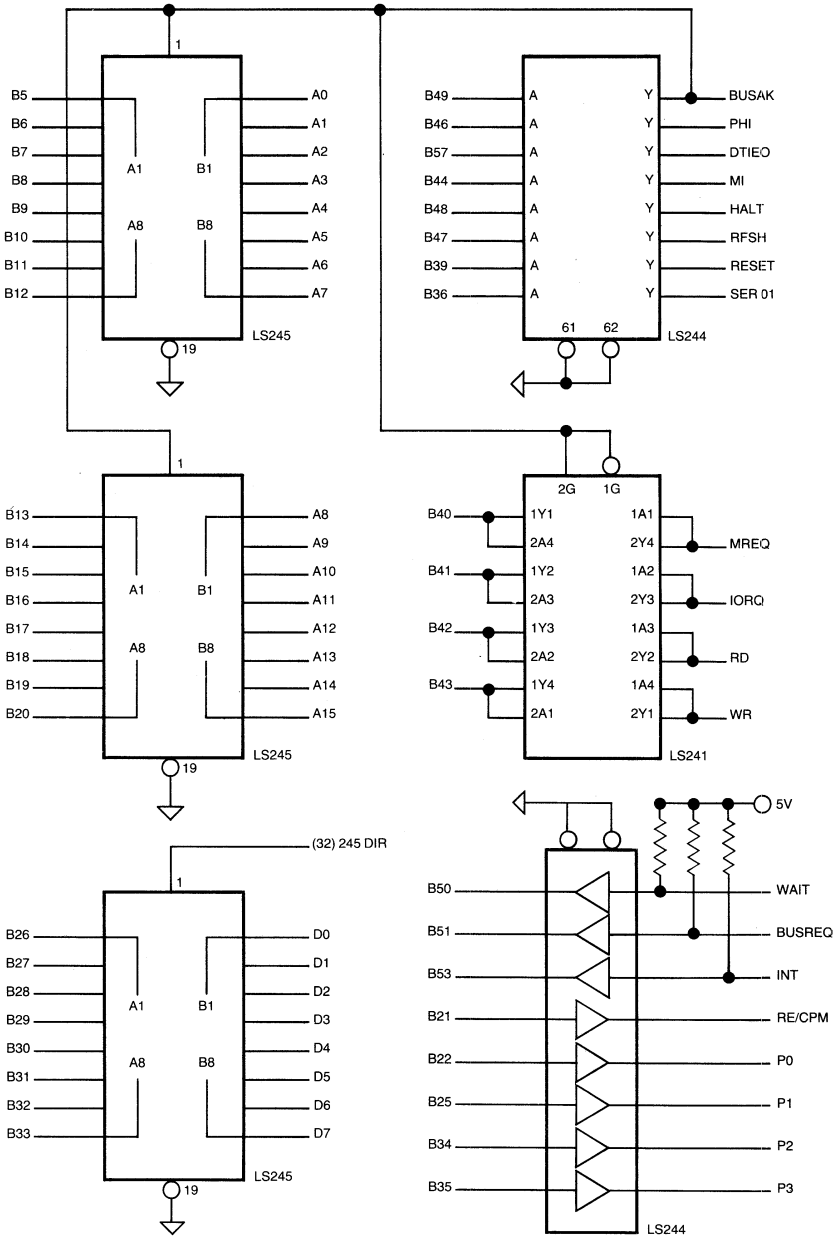
FULL GRAPHICS PROM SET

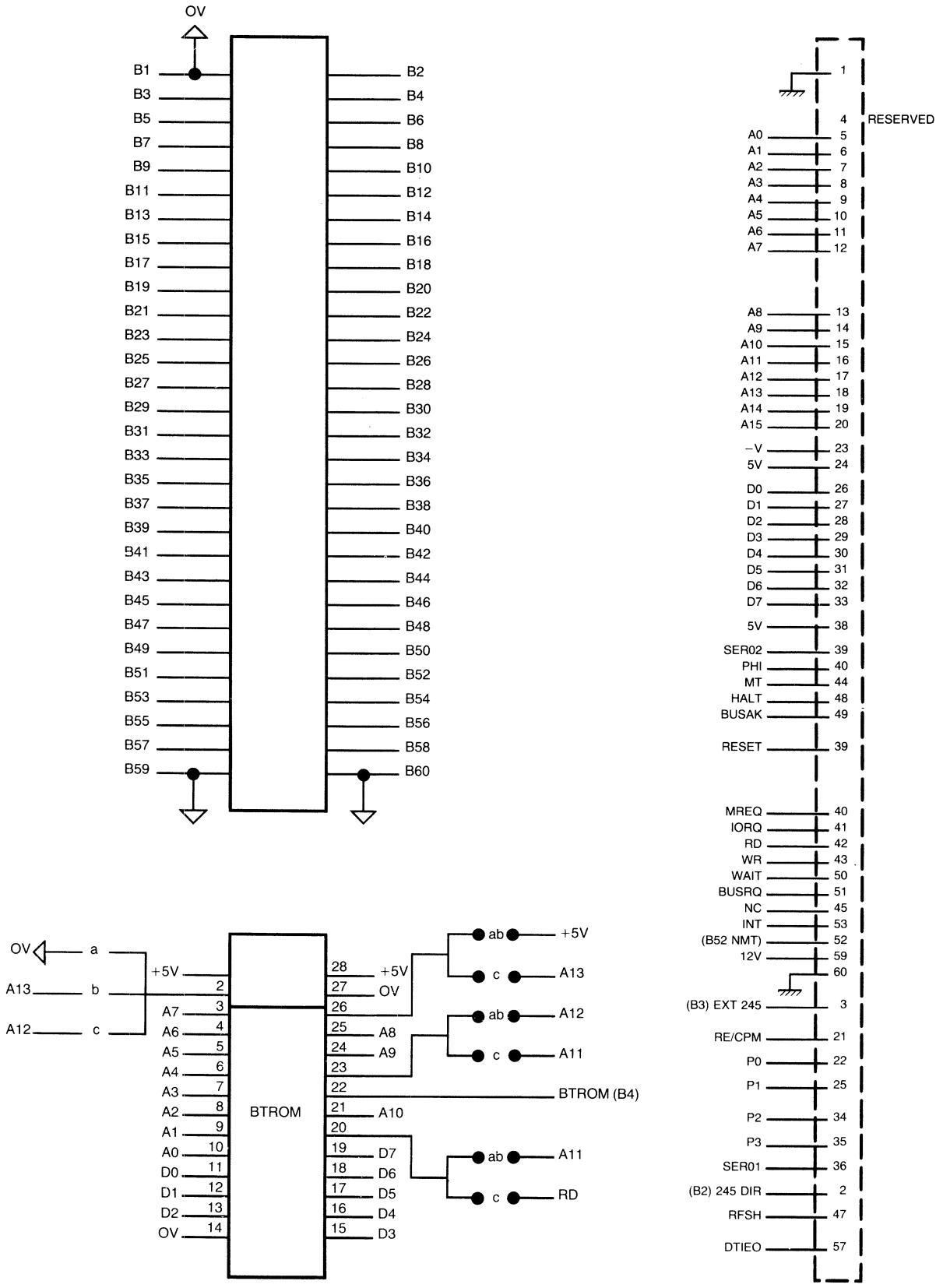


Chapter Four: MTX Bus Interface Card

MTX BUS INTERFACE

The MTX–SMI Bus Interface Card provides a buffered interface between the MTX and FDX units. Also situated on this board is the 64K Bootstrap ROM (see section on Bootstrap ROM).




OV
B1 B2
B3 B4
B5 B6
B7 B8
B9 B10
B11 B12
B13 B14
B15 B16
B17 B18
B19 B20
B21 B22
B23 B24
B25 B26
B27 B28
B29 B30
B31 B32
B33 B34
B35 B36
B37 B38
B39 B40
B41 B42
B43 B44
B45 B46
B47 B48
B49 B50
B51 B52
B53 B54
B55 B56
B57 B58
B59 B60
1
RESERVED 4
A0 5
A1 6
A2 7
A3 8
A4 9
A5 10
A6 11
A7 12
A8 13
A9 14
A10 15
A11 16
A12 17
A13 18
A14 19
A15 20
-V 23
5V 24
D0 26
D1 27
D2 28
D3 29
D4 30
D5 31
D6 32
D7 33
5V 38
SER02 39
PHI 40
MT 44
HALT 48
BUSAK 49
RESET 39
MREQ 40
IORQ 41
RD 42
WR 43
WAIT 50
BUSRQ 51
NC 45
INT 53
(B52 NMT) 52
12V 59
60
(B3) EXT 245 3
RE/CPM 21
P0 22
P1 25
P2 34
P3 35
SER01 36
(B2) 245 DIR 2
RFSH 47
DTIEO 57
OV a
A13 b
A12 c
+5V 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
D0 11
D1 12
D2 13
OV 14
BTROM
28 +5V
27 OV
26
25 A8
24 A9
23
22
21 A10
20
19 D7
18 D6
17 D5
16 D4
15 D3
ab +5V
c A13
ab A12
c A11
BTROM (B4)
ab A11
c RD

Chapter Five: Backplane

CONNECTOR PIN CONFIGURATIONS

J1 – Bus expansion connector

1	----	GND
2	Reserved	
3	Reserved	
4	Reserved	
5	<-->	A0
:	::::	:
:	::::	:
2;	<-->	A15
21	Reserved	
22	Reserved	
23	----	−12v
24	----	+5v
25		
26	<-->	D0
:	::::	:
:	::::	:
33	<-->	D7
34	Reserved	
35	Reserved	
36	Reserved	
37	Reserved	
38	----	+5v
39	--->	RES
40	<-->	MREQ
41	<-->	IORQ
42	<-->	RD
43	<-->	WR
44	--->	M1
45	<---	M-INH – On board Memory inhibit when low
46	--->	PHI – INVERTED
47	--->	RCY – internal refresh cycle
48	--->	HLT
49	--->	BUSAK
50	<---	WAIT
51	<---	BUSRQ
52	<---	NMI
53	<---	INT
54		KEY-WAY SLOT
55		
56		
57	--->	CTC-IEO
58		
59	----	+12v
60	----	GND

--->	OUTPUT FROM BOARD
<---	INPUT TO BOARD
<-->	BI-DIRECTIONAL LINE
----	DIRECT CONNECTION

Chapter Six: MTX–FDX Silicon Disc System

INTRODUCTION

Each FDX silicon disc module is capable of storing 256K Bytes of data. The modules are stackable to a depth of 32 boards representing a total of 8M Bytes per drive, Upto 4 drives may be supported by the controlling software. A silicon drive provides CP/M with an extremely fast form of bulk storage – a 128 Byte sector read is completed in about 500 microseconds, a write (with mandatory automatic verify) takes about 1 millisecond, there are no latency or settling times. The silicon disc modules have been designed to accept 256K Bit chips when they become economically viable.

SILICON DISC SUPPORT SOFTWARE – SIDISC.COM

Although the silicon disc hardware modules can be simply plugged into the backplane of any MTX-FDX computer system they still require software support, in exactly the same way as any other disc sub-system. This software is not yet available in prom and so, must be installed by the user every time the computer is switched on or reset. This is done simply by running the SIDISC program. SIDISC.COM contains the silicon disc handler code together with a small loader / installer program which supervises the installation and relocation of the handler software. This program must be run before CONFIGuring silicon drives into your system.

ADDING SILICON DISC MODULES TO YOUR SYSTEM

Once the modules have been physically installed (see the section on LINKS and SWITCHES) start your system up as usual. When you get the CP/M prompt issue the SIDISC command and check that the message states:

+ **SiDisc handler available for drives F,G,H & I:**
+ **Prom upgraded to version 4***

Where * represents your existing prom version number. If a message saying:

– **No memory space for SiDisc handler.**

is output then relocate your CP/M system size to at least 1K less. If a message saying:

– **Incompatible prom version already resident.**

appears then consult the manufacturers.

Assuming you get the right message use CONFIG to configure your silicon disc modules into CP/M's disc system. For example, if you have a single board linked for drive F then use:

A>CONFIG F:40

Or a 4 board set linked for drive F:

A>CONFIG F:43

You must now FORMAT the silicon disc. This is essential because when power is first applied to a silicon disc it will contain random junk alien to CP/M.

A>FORMAT F:

FORMAT will also check that the first 64K Bytes of your silicon disc are working OK. If not, an error message will be generated and you should double check your installation before consulting the manufacturer.

You're now ready to actually use the silicon disc. Try PIP'ing some files onto it – fill it up if possible so that STAT sees less than 64K Bytes of space remaining. If you get this far without any trouble then it's time to make the installation permanent:

Use STARTUP to force your system to run SIDISC at cold-boot time:

```
A>STARTUP SIDISC CONFIG anything-else-you-need-to-do
A>STARTUP
```

A second invocation of startup will setup your default CONFIGuration state. Now, whenever you switch on, your silicon disc will be ready for formatting. NOTE that formatting is only needed after switch-on NOT after every reset – formatting destroys all data stored on the disc – this will almost certainly not be desired after a reset when the silicon disc will still contain all its' old data. REMEMBER: the only time you need to format a silicon disc is after power on.

SILICON DISC CONFIG CODES

CONFIG CODE	NUMBER OF MODULES	TOTAL CAPACITY
40 =	1 module	256KB
41 =	2 modules	512KB
42 =	3 modules	768KB
43 =	4 modules	1MB
44 =	5 modules	1.3MB
45 =	6 modules	1.5MB
46 =	7 modules	1.8MB
47 =	8 modules	2MB
48 =	10 modules	2.5MB
49 =	12 modules	3MB
4A =	14 modules	3.5MB
4B =	16 modules	4MB
4C =	20 modules	5MB
4D =	24 modules	6MB
4E =	28 modules	7MB
4F =	32 modules	8MB

LINKS on the SIDISC BOARD

L1 & L2 are used to select which drive address (typically F:, G:, H: or I:) the silicon disc board responds to. The SIDISC software can support up to 4 silicon drives each of which may comprise up to 32 × 256 K silicon disc boards or 8 × 1Meg boards.

L1	L2	RELATIVE -- DRIVE -- PHYSICAL
OUT	OUT	0 F:
OUT	IN	1 G:
IN	OUT	2 H:
IN	IN	3 I:

SW1 is used to allocate a logical niche in the address space of a multi-board silicon drive. Each board in a multi-board drive must be given a unique slot in the total address space. This is done by switching one of the switches of SW1 ON, with the rest OFF, each board having a different switch selected. Furthermore the address space must be continuous, for example in a four board system one board must have SW1.1 ON, one must have SW1.2 ON, one must have SW1.3 ON and one must have SW1.4 ON. SW1 allows easy expansion for up to 8 disc boards in any one drive, however if more than 8 boards are required the scope of SW1 on the 9th and subsequent boards must be changed, this is done means of links on SKT2.

PIN 8	PIN 9	SW.1 ... SW1.8
TO P5	TO P4	BOARDS 1..8
TO P5	TO P6	BOARDS 9..16
TO P7	TO P4	BOARDS 10..24
TO P7	TO P6	BOARDS 25..32

Other links on SKT2 are used to configure the board to accept either 64K or 256K DRAM chips. For 64K devices connect:

P1 to P14
P2 to P13
P3 to P12
P10 to P11
Either P5 or P7 to P8
Either P4 or P6 to P9

For 256K devices connect:

P3 to P14
P4 to P13
P5 to P12
P10 to P11, P9 & P8

NOTE that when using 256K devices each silicon disc board holds 1MB of data and consequently only 8 boards may be configured into a drive. The scope of SW1 is therefore fixed.

The MPX links are provided to allow for possible timing differences in some DRAMS. The link is used to select different RAS/MPX delays and should normally be set to position '1'. Positions '3' and '5' extend the RAS/MPX delay further.

SISPOOL (SILICON PRINT SPOOLER)

SISPOOL.COM is a CP/M program which will run only on MTX computer systems equipped with SiDisc hardware. Its' function is to rapidly buffer up outputs to the CP/M LST: device effectively reducing print times by several orders of magnitude. The data is then sent on to the printer at the normal rate, in background, while CP/M continues to run unaltered in the foreground. Only processor dead-time is used for the background task, ie when awaiting or testing for keyboard entry. It should be noted that SISPOOL will not work with CP/M BIOS versions earlier than 07–04–83. The action of the spooler is totally transparent to the user and will work with any of the standard printer configurations of the MTX. Neither SISPOOL or its' data buffer will survive a coldboot or hardware reset. A safety feature of SISPOOL ensures that output is not redirected to a different physical device if the LST field of the IO byte is changed during a spooled printing session. In this event SISPOOL swaps – in its own local IO byte during spooled character outputs but leaves the newly assigned print device available to CP/M in the normal (unspooled) way. SISPOOL's local IO byte is only updated when its buffer empties. In this way it is possible to have two printers running simultaneously.

INVOKING SISPOOL

The resident SISPOOL driver software is automatically installed into high memory, above CP/M, when the SISPOOL command is first used. Note that SISPOOL will not load if the silicon disc handler software (SIDISC) is not resident or if there is no SiDisc hardware present. Once loaded, SISPOOL will remain active until the next COLDBOOT or system reset, unlike SIDISC which, of necessity, can survive COLDBOOT commands. The hardware requirement for SISPOOL is at least one SiDisc board (if 2 or more are present they will be made use of) which must be strapped for drive F: but which need not be fully populated. Before SISPOOL loads it sizes the silicon disc hardware and configures itself to use 64K, 128K, 512K, 1M, 2M, 4M OR 8M Bytes of space whichever is appropriate to the hardware installed – the memory must be continuous.

SISPOOL COMMANDS

Once SISPOOL has been successfully installed a number of supporting commands become available to enhance the usefulness of the package. These are:

SISPOOL S(top) Used to instantly stop data flow to the printer and erase all pending data.

SISPOOL P(ause) Used to instantly suspend data flow to the printer but leaves the data buffer intact. When paused any characters subsequently sent to the LST: device are passed on to the printer in the normal way, unspooled, 'short-circuiting' the spooler buffer.

SISPOOL R(esume) This command is used to restart spooled printing after a PAUSE command.

SISPOOL When used in this way, with SISPOOL already loaded, the command lists the current spooler status eg. PAUSE, BUFFER-EMPTY or IO-CHANGE.

THE IOBYTE, AND SISPOOL

Once a spooled printing session has been initiated, changes to the LST field of the IO byte are not allowed to affect the flow of spooled characters to the original LST: device. Instead spooled output remains un-redirected and unaffected – the original print device continues to be used to drain the buffer. However, subsequent characters sent to CP/M's LST: device are redirected to the new physical device but are not spooled – these transfers take place as if no spooler were present. That is until the spooler buffer is exhausted, when SISPOOL will automatically switch over to the newly selected physical print device.

Chapter Seven: Communications Board

INSTALLATION INSTRUCTIONS:

Providing that you closely follow the instructions below, you will be able to install your MTX communications board in approximately 10 minutes.

1 Ensure that your MTX is switched off and that all cables are disconnected.

2 Using the Allen key provided remove the three domed Allen head bolts from the right hand end plate of your MTX.

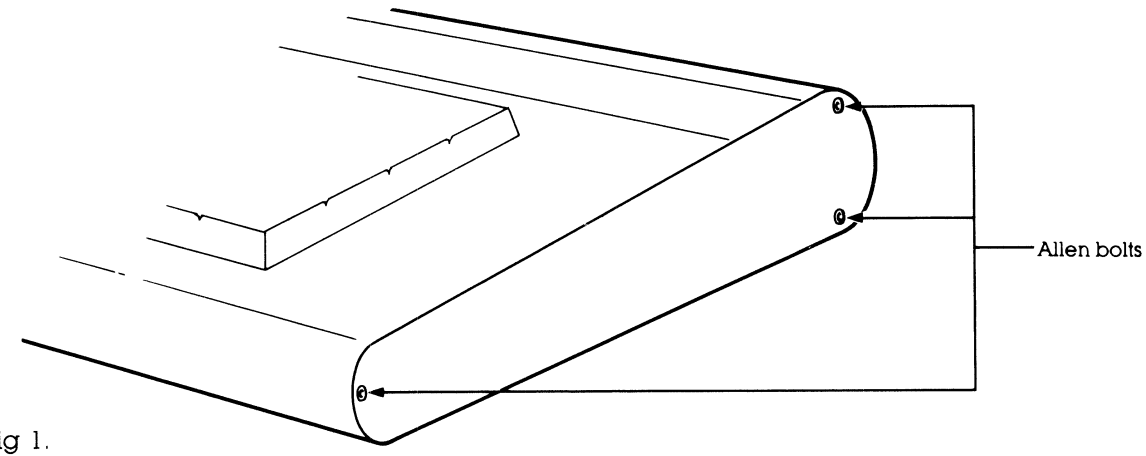


Fig 1.

3 Remove the bottom rear Allen bolt from the left hand end plate.

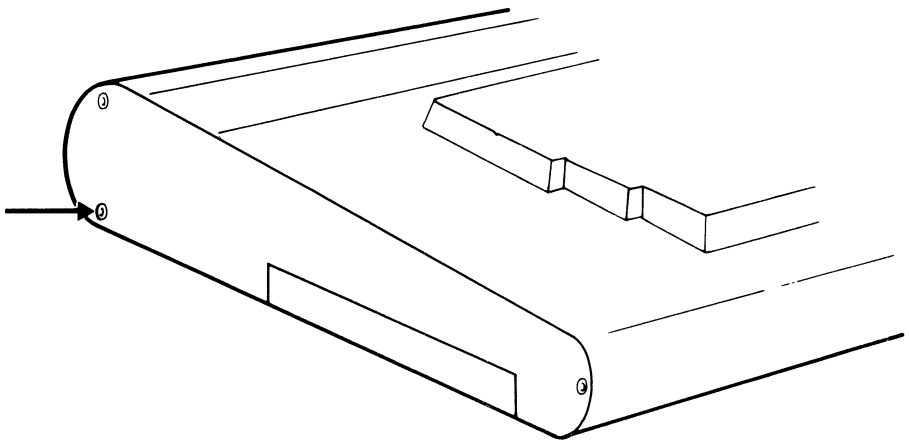


Fig 2.

4 Lift the MTX keyboard at the rear just above the plastic panel. The front is hinged and the unit will open like a clam shell. Be careful not to damage the keyboard interconnection cable.

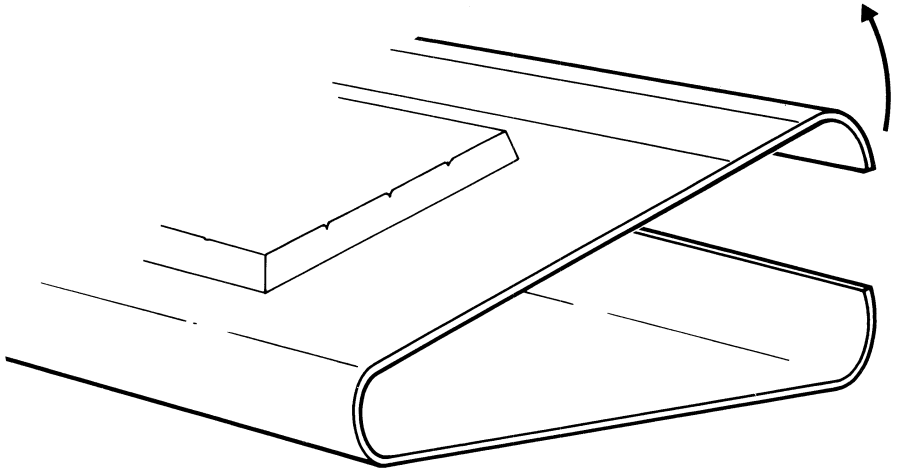
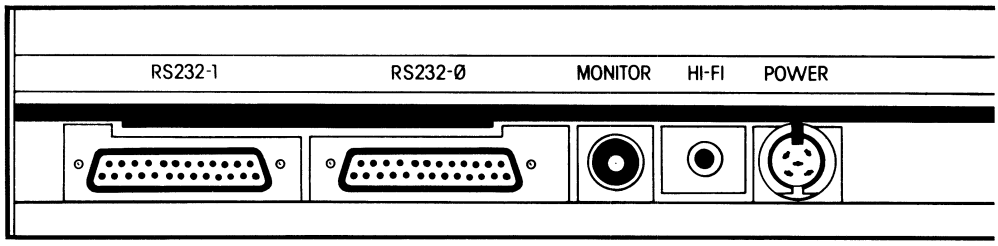


Fig 3.

5 Carefully push out the two plastic inserts occupying the apertures marked RS232–1 and RS232–0 on the rear panel.

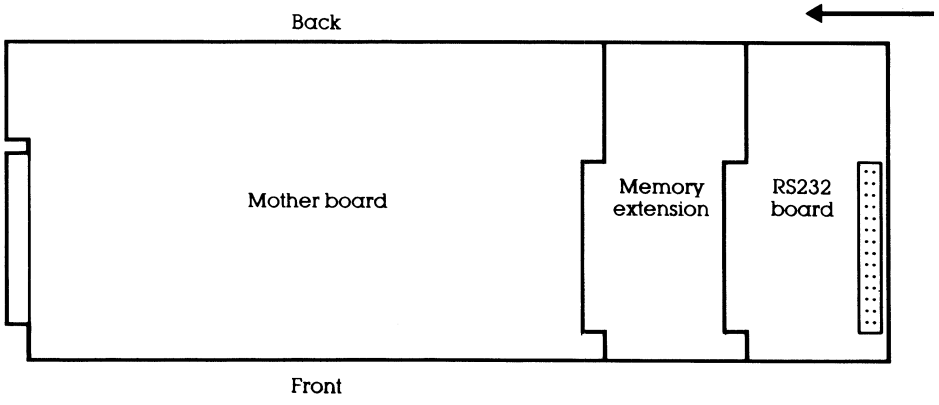
6 Look carefully at the two cables supplied with your system and pick up the cable which has only five conductors.

7 Place the 'D' type connector in the aperture marked RS232–0, mounting the 'D' type connector inside the MTX using the Allen bolts, nuts and washers provided. Ensure the connector has the wide edge at the bottom of the MTX.



8 Place the other cable in the aperture marked RS232–1, and secure as before.

9 Slide the RS232 card into the MTX so that the edge connector makes a firm connection with the motherboard (or RAM/ROM expansion if fitted).



10 Plug the cable with five conductors (RS232–0) into the header marked JA on the RS232 board. Ensure that pin 1 on the Molex connector goes to pin 1 on the Header.

11 Plug the cable with 8 conductors (RS232–1) into the header marked JB, ensuring that pin 1 goes to pin 1.

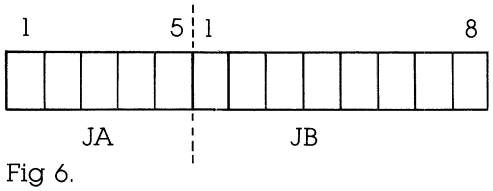


Fig 6.

12 Carefully close the MTX ensuring that all the cables are free from obstruction, and replace the end plates.

13 Your MTX now has its communications board fitted and is ready for use.

COMMUNICATIONS BOARD DESCRIPTION

The communications board incorporates a fully buffered 60 way bus for communicating with the MTX-FDX (floppy disc system), and twin RS232 ports.

The Zilog Z80 Dart (dual asynchronous receiver/transmitter), and the 1488/1489 line driver/receiver provides data transmission as specified by the electronics industries association standard RS232C.

CONNECTOR INFORMATION

J0 EDGE CONNECTOR

A		B			
$\overline{\text{GROM}}$	1	A0	+12	16	−V
A1	2	A2	0V	17	0V
A3	3	A4	$\overline{\text{RESET}}$	18	$\overline{\text{MREQ}}$
A5	4	0V	$\overline{\text{IORQ}}$	19	$\overline{\text{RD}}$
KEY	5	WAY	$\overline{\text{WR}}$	20	$\overline{\text{M1}}$
A6	6	A7	PHI	21	$\overline{\text{RFSH}}$
A8	7	A9	$\overline{\text{HALT}}$	22	$\overline{\text{BUSAK}}$
A10	8	A11	$\overline{\text{WAIT}}$	23	$\overline{\text{BUSREQ}}$
A12	9	A13	$\overline{\text{NMI}}$	24	$\overline{\text{INT}}$
A14	10	A15	CTCIEO	25	P0
D0	11	D1	P1	26	P2
D2	12	D3	P3	27	R0
D4	13	D5	R1	28	R2
D6	14	D7	$\overline{\text{RE}}$/CPM	29	SER 01
+5	15	+5	SER 02	30	0V

J1 HEADER

1	0V	21	$\overline{RE}$/CPM	41	IORQ
2	245 DIR	22	P0	42	RD
3	EXT 245	23	0V	43	WR
4	BTROM	24	0V	44	M1
5	A0	25	P1	45	0V
6	A1	26	D0	46	PHI
7	A2	27	D1	47	RFSH
8	A3	28	D2	48	HALT
9	A4	29	D3	49	BUSAK
10	A5	30	D4	50	WAIT
11	A6	31	D5	51	BUSREQ
12	A7	32	D6	52	NMI
13	A8	33	D7	53	INT
14	A9	34	P2	54	0V
15	A10	35	P3	55	0V
16	A11	36	SER 01	56	0V
17	A12	37	SER 02	57	DTIEO
18	A13	38	0V	58	0V
19	A14	39	RESET	59	0V
20	A15	40	MREQ	60	0V

RS232 CONNECTOR PIN DESCRIPTIONS

JA RS232–0 CHANNEL A:

CONTROL LINE	WIRE COLOUR	'D' TYPE CONNECTOR	INPUT/OUTPUT
1 $\overline{RXDA}$	Red	2	I
2 $\overline{TXDA}$	Orange	3	O
3 $\overline{DTRA}$/$\overline{RTSB}$	Yellow	5	O
4 $\overline{CTSA}$	Green	20	I
5 0V	Blue	7	

JB RS232–1 CHANNEL B:

CONTROL LINE	WIRE COLOUR	'D' TYPE CONNECTOR	INPUT/OUTPUT
1 TXDB	Black	2	O
2 RXDB	Brown	3	I
3 $\overline{DTRA}$/$\overline{RTSB}$	Red	4	O
4 $\overline{CTSB}$	Orange	5	I
5 $\overline{RIB}$	Yellow	6	I
6 $\overline{DTRB}$	Green	20	O
7 0V	Blue	7	
8 DCDB	Violet	8	I

CONTROL LINE DESCRIPTIONS

RXDA,RXDB	– Receive Data, (inputs,active high)
TXDA,TXDB	– Transmit Data, (outputs,active high)
DTRA,DTRB	– Data Terminal Ready, (outputs,active low)
CTSA,CTSB	– Clear To Send, (inputs,active low)
RTSB	– Request To Send, (outputs,active low)
RIB	– Ring Indicator, (inputs,active low)
DCDB	– Data Carrier Detect, (inputs,active low)

CONTROL LINE FUNCTIONS

JA3 and JB3 are connected to the same output driver. The driver input is link selectable to give either $\overline{\text{DTRA}}$ or $\overline{\text{RTSB}}$. Link A is factory set giving $\overline{\text{DTRA}}$. Channel A is configured as a data set, and Channel B is connected as a data terminal (input and output lines reversed).

The Channel A connector does not have all the handshake lines available from the DART. $\overline{\text{DTRA}}$ is a general purpose output whose level is set through bit 7 of write register 5 of Channel A. $\overline{\text{CTSA}}$ is the Transmitter Enable. This line is normally held in the enable condition by a pull up resistor. This allows the channel to operate under open loop conditions i.e. no handshake lines connected. A negative voltage on this input will halt the Channel A transmitter.

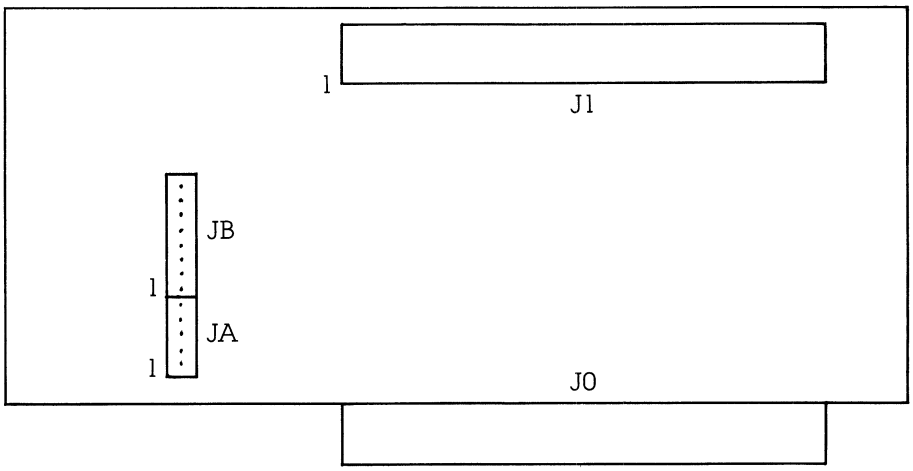
Channel B has all the available control lines except $\overline{\text{W/RDY}}$. RTS and DTR are general purpose output lines set through the channel B write registers. The inputs DCD and CTS are the receiver and transmitter enables respectively. Both are held in the enable conditions by pull up resistors. R1 is a general purpose input.

RING SYSTEM

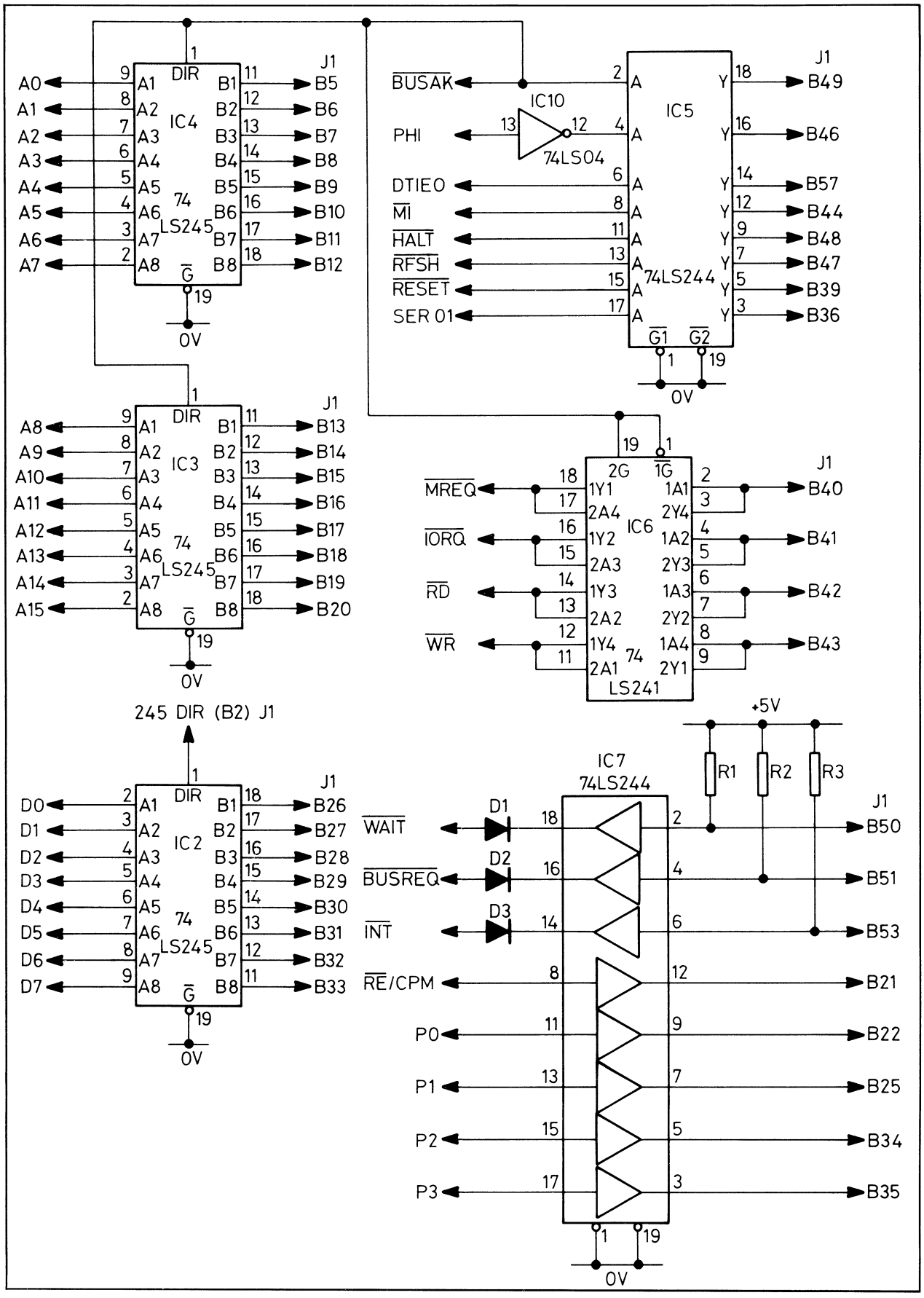
The MTX ring uses channel A of the dart. If the ring is installed, the baud command must not be used for either channel as the dart is initialised differently for the ring. Channel B is not used by the ring and is available as a serial I/O port. Node commands are provided to set the baud rate and data format for channel B.

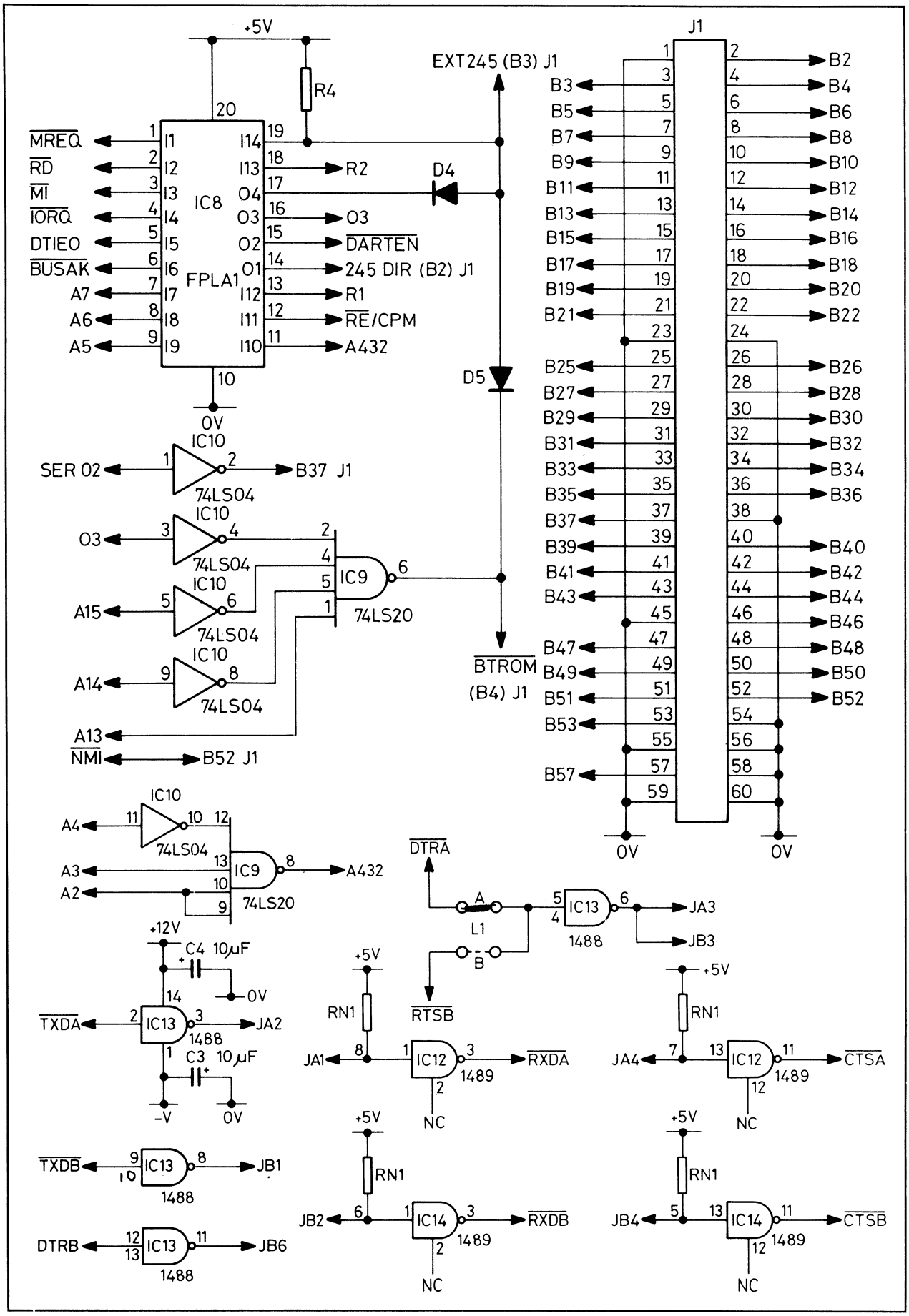
BOARD DESCRIPTION

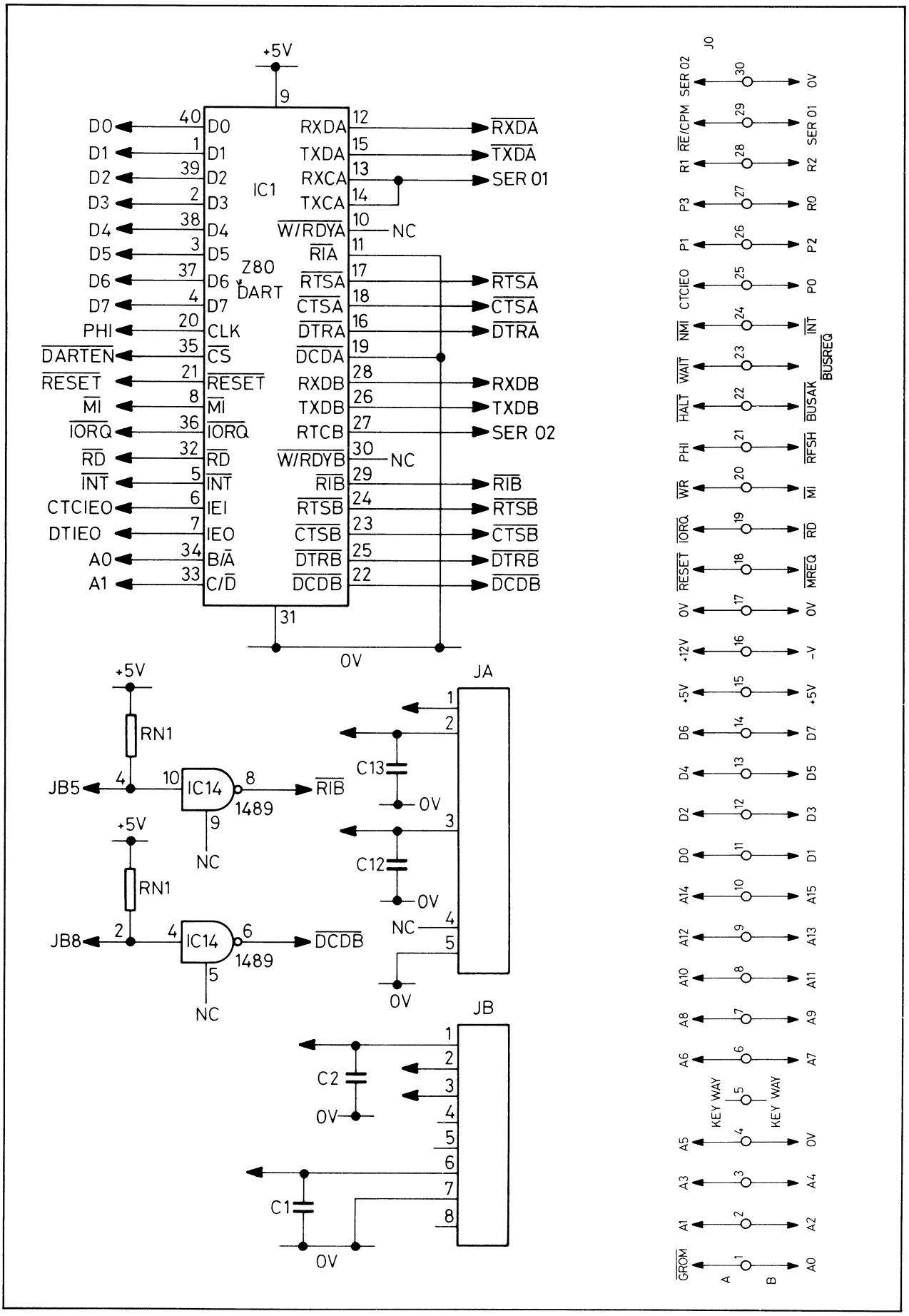
This board is added internally to the MTX. It incorporates a 60 way edge connector for communicating with the MTX motherboard; a 60 way header for communicating with the FDX (floppy disc system); and a 13 way header providing the twin RS232 ports.



COMMUNICATIONS BOARD CIRCUIT DIAGRAM




+5V
R4
20
MREQ
RD
MI
IORQ
DTIEO
BUSAK
A7
A6
A5
I1
I2
I3
I4
I5
I6
I7
I8
I9
IC8
FPLA1
I14
I13
O4
O3
O2
O1
I12
I11
I10
19
18
17
16
15
14
13
12
11
R2
O3
DARTEN
245 DIR (B2) J1
R1
RE/CPM
A432
10
0V
EXT245 (B3) J1
D4
D5
J1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14
B15
B16
B17
B18
B19
B20
B21
B22
B25
B26
B27
B28
B29
B30
B31
B32
B33
B34
B35
B36
B37
B39
B40
B41
B42
B43
B44
B45
B46
B47
B48
B49
B50
B51
B52
B53
B57
BTROM
(B4) J1
IC10
74LS04
SER 02
B37 J1
IC9
74LS20
A15
A14
A13
NMI
B52 J1
A4
A3
A2
A432
+12V
C4 10µF
C3 10µF
-V
TXDA
JA2
IC13
1488
TXDB
JB1
DTRB
JB6
DTRA
A
B
L1
RTSB
JA3
JB3
RN1
JA1
RXDA
IC12
1489
NC
JA4
CTSA
JB2
RXDB
IC14
JB4
CTSB


+5V
9
IC1
Z80
DART
D0
D1
D2
D3
D4
D5
D6
D7
PHI
DARTEN
RESET
MI
IORQ
RD
INT
CTCIEO
DTIEO
A0
A1
CLK
CS
IEI
IEO
B/A
C/D
RESET
RXDA
TXDA
RXCA
TXCA
W/RDYA
RIA
RTSA
CTSA
DTRA
DCDA
RXDB
TXDB
RTCB
W/RDYB
RIB
RTSB
CTSB
DTRB
DCDB
NC
SER 01
SER 02
0V
RN1
IC14
1489
JB5
JB8
JA
JB
C13
C12
C2
C1
J0
KEY WAY
GROM
BUSREQ
BUSAK
WAIT
HALT
NMI
CTCIEO
WR
IORQ
RESET
MREQ
RFSH
-V

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